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Concept Engineering GmbH

Concept Engineering Introduces RTLvisionTM PRO to Help Designers of IP-based System-on-Chip Reach Faster RTL Code Closure – New RTL debugging tool supports SystemVerilog, Verilog and VHDL standard languages

Free evaluation packages for RTLvision PRO are available from Concept's website at www.concept.de.

Concept Engineering announced the release of RTLvisionTM PRO, a customizable tool to help designers of intellectual property (IP)-based system-on-chip reduce the complexity of the debug process and makes it easier to understand and change register-transfer level (RTL) code. With the addition of RTLvision PRO to Concept Engineering's product line, the company now offers interactive visualization and debugging tools for all major design levels: RTL-level, gate-level and transistor-level.

Integrated circuit (IC), SoC, and field programmable gate array (FPGA) design and verification engineers who develop, integrate and debug RTL code and IP components are facing increasing productivity pressure as designs become more complex and challenging. Designers often alleviate this pressure by using IP-based SoC design methods. RTLvision PRO allows these designers to quickly understand, integrate and debug third-party or "inherited" IP.

RTLvision PRO helps engineers reach faster RTL code closure by enabling quick visualization of critical design fragments and easy understanding of design behavior and design miss behavior. With mixed-language support for System Verilog, Verilog and VHDL and ultra-fast HDL readers, RTLvision PRO can be used on today's most complex heterogeneous designs. This easy-to-use, high-performance tool helps reduce the complexity of the debug process via its interactive logic cone navigation feature, which shows just the critical portion of the RTL design in the logic cone window while concurrently providing links to the original source code.

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Concept Engineering Introduces SGvisionTM PRO to Help System-on Chip Designers Analyze and Debug Mixed-Mode Circuits

Tool provides detailed information for both digital and analog or library components

Concept Engineering announced the release of SGvisionTM PRO, a mixed-mode debugging tool that allows system-on-chip (SoC) designers and verification engineers to more quickly analyze and debug circuits that contain both digital and transistor-level components. SGvision PRO supports mixed-level debugging of SPICE and Verilog standard languages at the same time.

Many SoC implementation and debugging problems can be easily understood and solved when designers get detailed information and debug support not only from their pure digital components (Verilog), but also from the analog or library components (SPICE). Existing customers of the Concept's GateVision® PRO (for gate-level debugging) and SpiceVision® PRO (for transistor-level debugging) tools had been requesting

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