December, 11 — 12

electronic design automation Forum08

edaForum08

Hilton Hotel
Dresden, Germany

www.edacentrum.de/edaforum/

Content

Preface

For more than forty years microelectronics has always been marked by fast innovations happening in short time. The most important progress is based on the success of the microelectronics industry by exponentially reducing the feature sizes and thereby doubling the amount of components per chip every two to three years. The most important trend resulting from this are the exponentially falling prices for the particular functions, which in turn has led to enormous improvements of the economical productivity of the entire industry influencing almost every area of our daily lives. In order to optimize the microelectronic products for their corresponding applications, application-oriented electronic design automation is decisive.

edaForum08 is well aware of these challenges and is ready to tackle them. Therefore we have invited experts from the USA, Asia, and Europe to share with you newest design methods allowing to design more and more complex products in short time, but with high efficiency and highest quality. However, edaForum08 is much more than that. It sticks to its principles and offers besides the technical talks also space and time for today's burning economical questions of microelectronics starting with the first keynote discussing the role of fabs and current trends of fabless design. Further topics will give you details on economical chances of "More than Moore", which are of especially high importance for the German automotive electronics.

On a larger scale we also would like to discuss highly important aspects of microelectronics and EDA for the global world economy and vice versa.

First and foremost we should talk about global warming on the one hand, and fossil fuels coming to an end on the other hand, but all these problems don't only bear risks and therefore shouldn't only be seen as bleak. Indeed, there are also many new opportunities for microelectronics. Due to its importance we have dedicated an entire session of the edaForum08 to this question. In this context we also seize the opportunity to discuss further topics, such as aging societies and the shortage of young engineers and computer scientists. A second keynote and a thrilling panel will conclude our Forum this year.

During and in-between the sessions we appreciate lively discussions and welcome your ideas and questions.

So I'm looking forward to welcome you to this year's edaForum in Dresden!

Wolfgang Rosenstiel
Chairman edacentrum

Simon Yang, Chartered Semiconductor Manufacturing

Design and Process Interactions at the 32nm Node and Virtual IDM Environment

As we arrived at the physical limits of CMOS technology, conventional scaling methodology is no longer viable to maintain the technology progress on the traditional trend characterized by Moore's Law. On the other hand, due to the proven SOC integration capability and the convergence of applications on hand-held platforms, the appetite of the market for more transistors in a chip, lower power consumption, and faster operation speed at lower cost is far from tamed. As a result, the need for innovation in the semiconductor industry intensified in recent years. High K metal gate materials, air-gap interconnects, and EUV lithography are the examples of the newest technologies in play which were not considered in the realm of reality just a few years ago.

It becomes more important and urgent than ever for product design members in fabless community to have intimate understandings of process technologies, even during the early stages of technology R&D. This is because that: (1) Most of the new technologies have not only strong interactions with design styles in the area of manufacturing robustness (the traditional issues covered by DFM) but also design restrictions/guidance for achieving the promised product performance gains; (2) It is necessary in order to compete with leading IDMs in term of Time-To-Market. For years, good IDM companies have practiced simultaneous technology development and product design through close communication among the groups and certain build-in elasticity in the infrastructure to achieve rapid volume ramp after the qualification of each new technology node. The foundry-fabless arrangement historically lags leading IDMs in this ramp by >2 years due to the sequential nature of process technology development, circuit IP design and verification, and product design and qualification. This situation was somewhat tolerable largely because they were playing in different application markets. The dynamics will certainly change when the applications start to converge onto a common platform. EDA industry is clearly positioned to play a vital role in addressing these opportunities during the exciting period.

In this talk, we will first report, from the view of semiconductor technology and manufacturing specialists, the current status of Moore's Law and our pursuit for "More Moore" and "More Than Moore". The technology innovation and the resulting breakthroughs highlighted are targeted to underpin the joint development in New York among IBM, STM, Freescale, Infineon, Samsung, and Chartered and the design enablement and manufacturing infrastructure accessible to the fabless community through the Common Platform manufacturing and enablement alliance of Chartered, IBM, and Samsung. Special focus will be given to the recently announced breakthrough 32nm technology with the introduction of High K Dielectric and Metal Gate.

Thursday, Dec. 11, 2008
1:30 pm — 2:30 pm
Saal 1

Specific examples (such as gate capacitance vs gate leakage and Vt variation vs transistor gate area) will be described to demonstrate the critical breakthrough of the "physics limits" under traditional scaling methodology. Since all of this technology prowess will be for naught if the entire design infrastructure and enablement eco-system is not brought to the same level of sophistication and capabilities, the business constructs of the entire ecosystem surrounding the technology will then be described, including a brief exploration of how this model has evolved over time. A brief description of some of those EDA systems attuned to the 32nm technology currently being deployed will also be given. Lastly, we will talk about the need for the so called virtual IDM collaborative work infrastructure among foundry, IP vendors, and fabless companies to improve time-to-market at new technology introductions, together with some discussions on the possible methodologies to achieve that.

Simon Yang
Chief Technology Officer
Senior VP for Fab Operations
Chartered Semiconductor Manufacturing

Dr. Simon Yang joined Chartered in October 2005 where he is responsible for developing and driving strategic programs in support of Chartered's corporate objectives and long-term strategic direction.

Dr. Yang brings more than 20 years of experience in the semiconductor industry. He previously held key positions in technology development and advanced fab operations. He was a senior vice president for logic technology development and manufacturing at Semiconductor Manufacturing International Corporation (SMIC) and prior to that, a director of logic device and process integration at Intel. Prior to joining Chartered, he was president and CEO of Ciwest, a semiconductor start-up based in China.

Dr. Yang has been awarded more than 12 U.S. patents and is the author or co-author of more than 30 technical papers. He holds a bachelor's degree in electrical engineering from Shanghai University of Science and Technology, and a MS in physics and Ph.D. in materials engineering from Rensselaer Polytechnic Institute in Troy, New York.

"GO YOUR OWN WAY" - More Than Moore & Less More Moore for Commercial Success

Session Keynote:

Pietro Perlo, Fiat

Energy Savings by Essential System Integration in the Forthcoming E-Mobility

The electrical power-train is superior to the direct combustion based propulsion from several points of view: better overall energy efficiency, lower emissions, better fun to drive and reduced use of primary materials. The power-train of a full Electric Vehicle (EV) is conceptually the simplest and the most economic; there are no technical, economical, social or environmental reasons against its adoption.

Full Electric Vehicles require high efficiency power electronics to connect the various stages including the e-grid (or local renewable energy sources), accumulators, high power-energy switches, in the vehicle high power lines, high power converters, drivers and e-motors. Rather than more electronics or more computational power the development of higher efficiency electronic subsystems and, even more important, the engineering of their globally optimized integration-management, will be the factors to speed-up towards this new exciting era of mobility.

Pietro Perlo
Director and Senior Scientist
Centro Ricerche Fiat

Pietro Perlo took his Laurea degree in General Physics at the University of Torino in 1980. In the mid 90', he originated the first world-wide commercial introduction of diffractive and microoptics into the automotive, motorcycles, general lighting and IR systems for intrusion alarm. Pietro coordinates the Italian programme on the development of microcombustion based range extenders. As director and senior scientist at Centro Ricerche Fiat, he concentrates his interests on the optimal integration of enabling technologies and systems for zero emission mobility. Pietro is the Chairman of the Working Group Automotive of the EU Technology Platform EPoSS on Smart Systems Integration.

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2:35 pm — 3:20 pm
Saal 2

Successful companies are special somehow, they go their own way. While 'More Moore' is no longer special, 'More than Moore' offers a lot, to let everybody find his own way.

Claudio Contiero, STMicroelectronics

Progress and Challenges in Semiconductor Mixed Technologies for Smart Power Applications

Increasingly attention is paid to the "More-than-Moore" trend where the progresses on "digital" and real "analog world" interfacing do not depend merely on technology node evolution like in the digitally centric "Moore's Law". Mixed power technologies like Bipolar-CMOS-DMOS (BCD) represent a good example of this concept. They offer high voltage and current capability, analog and digital functions, large flexibility through a large variety of integrated components on technology nodes moving with years of delay with respect to advanced CMOS. The on-chip coexistence of so different functions faces many challenges: from the existing EDA tools not always adequate to address the peculiar needs, to the robustness and reliability requirements more and more demanding especially for automotive applications. In addition the growing push on price reduction requires a growing efficiency in developing more effective technologies than in the past.

This presentation will provide an overview about the more recent BCD development trends and challenges on technology, design tools aspects, approaches and methodologies for an early, complete but fast reliability characterization.

Claudio Contiero
Technology R&D
Director - Smart Power Technology
Competence Center
STMicroelectronics Srl

Claudio Contiero is Director of Smart Power Technology Competence Center in STM´s R&D Labs of Milano, Italy. He graduated magna cum laude in Physics at the University of Padova in 1976. In 1978 he joined SGS-ATES (now STM), pioneering the introduction of a new integrated silicon technology, called "BCD" in 1983 and contributing to its extension from 20V to 700V and evolution from the 1st (4 µm) to the 8th (0.18 µm) generation. Mr. Contiero is co-holder of many patents and coauthor of many technical papers in the field of semiconductor power technology. He has served several times as technical committee member of various international Symposia and Conferences, reviewing papers and giving many invited talks. In 2006 he has been the "Technical Program Chairman" in the IEEE – Int. Symp. on Power Semiconductor Devices & ICs. He is a member of the IEEE EDS Power Devices and ICs Technical Committee.

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4:00 pm – 4:30 pm
Saal 2

"GO YOUR OWN WAY" - More Than Moore & Less More Moore for commercial success

Stephan Guttowski, Fraunhofer IZM

Technology Aware Modelling for Automation in Physical Design of Heterogeneous Systems

While system-on-chip (SoC) and PCB design teams are operating with highly developed EDA tools, there is a lack of automation tools for the design of heterogeneous systems. This is particularly true for the engineering of so called 2.5D SiP, which integrate heterogeneous components (IC's, passives etc.) over several vertical layers/modules. For these systems component placement today is a time consuming task. Even more important is the lack of a tool support for technology selection.

In this talk a new methodology for component autoplacement for folded and stacked 2.5D SiP integrated with technology selection on an objective basis is presented. A design approach that is based on the simultaneous consideration of numerous layout solutions will be shown and demonstrated. The structuring of physical design, a novel modelling of technological components for folded and stacked 2.5D SiP, and sketch algorithms for technology constrained automated placement, based on multicriteria optimization, will be discussed. Together with a multicriteria decision support tool this results in a novel design approach for heterogeneous systems.

Stephan Guttowski
Dep. System Design & Integration
Fraunhofer IZM

Dr. Stephan Guttowski obtained his M.Sc. degree in EE from in 1994 and his Ph.D. degree in 1998 from the Technical University Berlin. From 1998 to 1999, Dr. Guttowski worked as a Post Doctoral Research Fellow at the Massachusetts Institute of Technology (M.I.T.) in Cambridge, USA. In 1999, he joined the Research Laboratory for Electric Drives at DaimlerChrysler AG in Berlin. Dr. Guttowski started to work with Fraunhofer IZM Berlin in October 2001. From 2002 to 2005, he headed the Advanced System Development Group. Since January 2006, he has been head of the department of System Design & Integration. Dr. Guttowski is a member of the Association of German Electrical Engineers (VDE) and the Institute of Electrical and Electronics Engineers (IEEE).

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4:30 pm — 5:00 pm
Saal 2

Successful companies are special somehow, they go their own way. While 'More Moore' is no longer special, 'More than Moore' offers a lot, to let everybody find his own way.

Christian Sebeke, Bosch

As good as it gets - How much more EDA needs "More than Moore"?

More components, such as analog/radio frequency (RF), passive, high voltage (HV) power, sensor/actuator, bio-chip and micro-electro-mechanical system (MEMS) will be added to pure CMOS; processed or embedded in the chip or package instead of being added at system level. This takes system integration including software to the next level and challenges mixed-mode design with demand for high performance system level design, verification, validation, simulation and modelling with formalised or even executable specifications and others. Facing the situation, design methodology groups demand a specific roadmap from EDA vendors, to enable leverage from technology advances. They envision a shift from today's bottom-up to a top-down approach. But is everybody ready to jump on that train?

This talk will give a perspective on what will happen facing all challenges on the background of the field of forces around EDA which is spanned by methodology, users, customers and vendors.

Christian Sebeke
Section Manager
Design Methodology Group
Automotive Electronics
Robert Bosch GmbH

Dr. Christian Sebeke received the Dipl.-Ing. and the Ph.D. degrees from the University of Hannover in Germany 1990 and 1996, respectively. He joined Philips Semiconductors in Switzerland, 1995, dealing with all aspects of packaging, test, front-end and back-end design. From 2001 though 2005 he held technical marketing and marketing management positions with Agilent Technologies SOC Test Division, now Verigy, and Philips LCOS. Dr. Sebeke joined Robert Bosch GmbH in 2005, where he is responsible for design methodology which has the practical aspect of technology transfer from international tool vendors, research institutes and universities to the design teams. Topics range from digital to analog and mixed-signal, in front-end and backend, touching test, QA as well as manufacturing with the specific requirements on automotive quality and reliability.

Thursday, Dec. 11, 2008
5:00 pm — 5:30 pm
Saal 2

"WHAT A WONDERFUL WORLD" More (Green) Chips for Less CO_2

Session Keynote:

Gerd Teepe, AMD Saxony

Performance per Watt – Mission for Architecture and Design in Computing

High Performance Computing is reaching power limits. The energy bill of a computing center over its lifetime is surpassing the cost of its initial computer equipment purchase. "Performance per Watt" is now the new paradigm in compute-architectures, modes of operation, and design methodology, in view to avoid an imminent energy crisis in computing.

The ever continuing momentum however, for next generation deep submicron technologies beyond 45 and 32 nanometer, complements the power reduction design strategies on the drawing board today. However, the right technology and design choices cannot be made without the strong support from the EDA industry, as the time-window for implementation of new power saving methodologies is very short. In addition, the high system complexity is forcing a close cooperation of all system partners beyond component optimization of CPU, memory, I/O and power supplies.

This talk will outline IC design strategies for computing chips and describe system and technology considerations for next generation power-aware computing solutions.

Gerd Teepe
Director Dresden Design Center
AMD Saxony

Dr. Gerd Teepe is heading the Dresden Design Center for AMD Saxony in Dresden, Germany.

Dr. Teepe studied electrical engineering at the RWTH Aachen University, concluding with a Ph.D. in 1986. From then on he has been with the semiconductor industry, first with NEC in Tokyo, Japan, where he carried out research in fault-tolerant micro-architectures. Before joining AMD in 2004, Dr. Teepe has been with Motorola-Semiconductors in the following functions: IC-Design Engineering, IC-Design Management, as well as Marketing- and Operations-management. In his last position he was heading the "Strategy and Advanced Systems Labs" in Munich and Detroit, chartered to develop the strategy for the entire automotive semiconductors business unit of Motorola. In his career with Motorola, Dr. Teepe has been working out of Geneva, Toulouse and Munich with reports from Austin, Detroit and Tokyo.He holds over 50 formal publications. In addition he is vice-chairman of the GMM microelectronics engineering association, which is part of German VDE/VDI.

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2:35 pm – 3:20 pm
Saal 1

Wouldn't it be wonderful to enjoy all conveniences of our modern life while having neither energy consumption nor CO_2 emission? – Green chips may surely are a step on the way towards it.

Volker Kiefer, Qimonda

Energy Efficiency in DRAM

Energy efficiency in electronic systems is a dominant topic in our industry. Among many other components, almost every electronic system contains memories and specifically DRAMs. Their energy consumption depends on the target application.

The Si technology used to manufacture a DRAM provides an important lever for optimizing its energy consumption. This is independent of its final application market. Smart circuit design can also contribute significantly to energy saving. Here, applications drive the implementation goals. For example, energy consumption in standby mode typically is crucial for mobile devices, whereas server applications demand reduced power in active mode. Innovative circuit development addresses these different goals. Furthermore, EDA forms a crucial base technology for enabling energy efficient designs.

This presentation will provide an overview of DRAM's contribution to energy efficiency and the required next steps for further improvement.

Volker Kiefer
Vice President for CAD
and Software Development
Qimonda AG

Volker Kiefer is Vice President for CAD and Software Development at Qimonda. His responsibilities include definition, implementation and maintenance of the Qimonda DRAM design flow, software development, resolution enhancement techniques and TCAD. After receiving his diploma in Computer Science in 1991 from TU Munich, he worked at Motorola in Germany and in the US, holding ASIC and CAD engineering positions. In 1997 he joined Siemens/Infineon in the DRAM Development Alliance in Burlington, VT. Since then he has led design and CAD teams in the US and Europe within Infineon's Memory Products business unit, which became Qimonda in May 2006.

Thursday, Dec. 11, 2008
4:00 pm — 4:30 pm
Saal 1

"WHAT A WONDERFUL WORLD" More (Green) Chips for Less CO_2

Piet Demeester, Ghent University

ICT: A Big Energy Consumer

Computers, televisions, internet, mobile phones and many more information and communication technologies (ICT) and devices have become an essential part of our lives. A major challenge for the coming decades is the operation of all this ICT equipment in a sustainable way. Today the operation of ICT equipment is responsible for about 2% of the total energy consumption worldwide, not including the energy consumption during the manufacturing and the disposal phase. Effort in different directions started to reduce this energy footprint of ICT. Examples are energy efficient servers and cooling solutions, advanced (optical and wireless) networking technologies, energy optimized content and application management, etc. Of course ICT is also an enabler against the depletion of natural resources and global warming (e.g. teleconferencing, building automation, intelligent transport systems, process control and many more). This talk will primarily focus on the energy consumption of ICT.

Piet Demeester
Department of Information Technology
Ghent University

Dr. Piet Demeester received his Ph.D. degree (1988) at Ghent University, where he became professor in 1993. He is heading a research group with over 100 members (www.ibcn.intec.ugent.be). His current research interests include: multilayer networks, Quality of Service (QoS), mobile and sensor networks, access networks, grid computing, energy efficient ICT, distributed software, network and service management, techno-economics and applications. He is co-author of over 700 publications in international journals or conference proceedings and received multiple scientific awards. He is member of the management board of IBBT (www.ibbt.be) and heading the iLab.t infrastructure lab (ilabt.ibbt.be).

Thursday, Dec. 11, 2008
4:30 pm — 5:00 pm
Saal 1

Wouldn't it be wonderful to enjoy all conveniences of our modern life while having neither energy consumption nor CO_2 emission? – Green chips may surely are a step on the way towards it.

Gerhard Fettweis, Technical University of Dresden

How to Design Really Low-Power Cellular Systems

Chipset design for cellular communications has a long tradition of creating low-power system solutions for handsets. As the energy cost for running the infrastructure network is increasing dramatically, new total system solutions are necessary. How can we design from gate to chip to network element to system solutions? A set of new approaches and challenges shall be addressed, paving the path for a complete new design methodology for future "cool silicon".

Gerhard Fettweis
Head of the Vodafone Chair
Mobile Communications Systems
Technical University of Dresden

Dr. Gerhard Fettweis studied Electrical Engineering at the University of Technology (RWTH) Aachen and earned his Ph.D. degree at the same university in 1990. From 1990 to 1991, he was Visiting Scientist at the IBM Almaden Research Center in San Jose, CA, developing signal processing innovations for IBM's disk drive products. From 1991 to 1994, he was a Scientist with TCSI Inc., Berkeley, CA, responsible for signal processor development projects for cellular phone chip-sets. Since 1994 he holds the Vodafone Chair at the Technical University of Dresden, Germany. During this time, next to producing scientific innovations, he has founded six start-ups: Systemonic (today NXP Semiconductors), Radioplan (today Actix), Signalion, InCircuit, Dresden Silicon (today Signalion), and Freedelity.

Dr. Fettweis is an active member of the scientific community in general, also organizing conferences (e.g. TPC Chair of ICC 2009) and research projects. His research focuses on new wireless communications, systems for cellular and short range networks, and hardware/software implementation architectures.

Thursday, Dec. 11, 2008
5:00 pm — 5:30 pm
Saal 1

Daniel D. Gajski, University of California at Irvine

New Strategies for System Design

With complexities of Systems-on-Chip (SOCs) rising almost daily, the design community has been searching for a new methodology that can handle given complexities with increased productivity and decreased time-to-market. The obvious solution that comes to mind is increasing levels of abstraction, or in other words, increasing the size of the basic building blocks. However, it is not clear what these basic blocks should be and what should be the strategy for creating a SOC out of these basic blocks. To make things more difficult, the difference between software and hardware is becoming indistinguishable which, in turn, requires sizable change in the industrial and academic infrastructure.

In order to find the solution, we will look first at the system gap between SW and HW designs and derive requirements for the system design flow that includes software as well as hardware. In order to enable new tools for model generation, simulation, synthesis and verification, the design flow has to be well defined with unique abstraction levels, model semantics and model transformations that correspond to design decisions made by designers. We will introduce the concept of model algebra that supports this approach and can serve as an enabler for the extreme makeover of system design and, consequently, system industry. We will support this concept with hard data and finish with a prediction and a roadmap towards the final goal of increasing productivity by several orders of magnitude while reducing expertise level needed for design of billion-transistor systems to the basic principles of design science only.

Friday, Dec. 12, 2008
8:45 am — 9:30 am
Saal 1

Daniel D. Gajski
Center for Embedded computer Systems
University of California at Irvine

Dr. Dan Gajski, a leader in the areas of embedded systems, design methodologies and languages, headed the research teams that created new design methodologies, tools and languages. He was instrumental in developing formalisms and algorithms for high-level synthesis, the definition of the finite-state-machine with data (FSMD), system level languages such as SpecCharts and SpecC, and design tools such as SpecSyn and System-on-Chip Environment. Many of these concepts have been adapted by academia and industry in the last 25 years.

Dr. Gajski directs the UCI Center for Embedded Computer Systems, with a research mission to incorporate embedded systems into automotive, communications, and medical applications. He has authored over 300 papers and numerous textbooks, including Principles of Digital Design (Englewood Cliffs, NJ: Prentice Hall, 1997) that has been translated into several languages.

He holds Dipl.-Ing. and M.S. degrees in electrical engineering from the University of Zagreb, Croatia, and a Ph.D. in computer and information sciences from the University of Pennsylvania, Philadelphia. After 10 years as Professor at University of Illinois he has joined UCI, where he presently holds The Henry Samueli Endowed Chair in Computer System Design.

"LET'S TWIST AGAIN"
More Future in Microelectronics

Session Keynote:

Brian Matas, IC Insights

IC Industry Review and Forecast — Light at the End of the Tunnel

Historically, the semiconductor market has been characterized by a pattern of cyclical peaks and valleys. Though the exact duration and magnitude of moving from one phase to the next has always been difficult to predict, there are some key elements such as worldwide GDP growth, electronic system sales growth, IC unit volume shipments, and capital spending trends that have suggested when a cycle is bottoming or peaking. Whether in a peak or valley, the IC industry continues to relentlessly develop smaller, faster devices with greater density that consume less power for an ever-growing list of applications. Though dour economic conditions suggest that the IC industry is in a weak period, it is often during cyclical downturns that some of the brightest innovations and biggest gains are made.

This presentation will provide a review of the semiconductor market history and forecast and present IC Insights' perspective of where the industry is currently positioned in its cycle. Included in the presentation is IC Insights' view on why it believes "fab-lite" companies, fabless companies, and pure-play foundries are on a collision course. Despite this and the softness in the current market, IC Insights believes that the outlook for the IC market is bright.

Brian Matas
Vice President, Market Research
IC Insights, Inc.

Brian Matas has worked in the semiconductor industry for more than 20 years. At IC Insights, Mr. Matas specializes in analyzing and forecasting developing trends in the analog, microcontroller, microprocessor, and memory IC markets. Additional responsibilities include monitoring IC trends in consumer electronics. Prior to helping form IC Insights, he worked several years with Motorola in process engineering and with ICE Corporation in market research analysis.

Mr. Matas received his Bachelor's degree in Physics from Anderson University and a Master's degree in aeronautical science from Embry-Riddle Aeronautical University Daytona Beach.

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9:35 am — 10:20 am
Saal 2

Barbara Schaden, Infineon

How About the Linkage Between Microelectronics and Global Economy?

It is well known that the microelectronic industry is closely correlated to the development of the world economy. It proves that volatility and growth of the semiconductor industry are not only caused by an industry-specific, technologically determined product cycle, but are also highly influenced by the macroeconomic environment. Correlation between both increased and is a result of the proceeding commoditization. A change in global economic growth directly affects the demand for semiconductors via changes in private consumption and expenditures of organizations. Additionally, the so-called global megatrends like shortage of natural resources, ageing society, increasing mobility and urbanization influence the microelectronics industry.

The presentation will highlight current developments and future trends which will have an observable impact on the microelectronics industry.

Barbara Schaden
Director & Chief Economist
Corporate Development
Infineon Technologies AG

Dr. Barbara Schaden started her professional career at the Ifo Institute for Economic Research in Munich. From 1994 to 1998 she worked in the Dresden branch. Dr. Schaden then continued her career in Munich with responsibility for the field Structural Analysis (1998 to 1999) and joined the Ifo Institutes' Economic Analysis and Forecasting team soon thereafter. She was the Ifo representative in the German tax estimation working group. In 2001, she joined the Corporate Strategy Department of Infineon Technologies AG. She holds the position of a Chief Economist responsible for Economic Analysis and Forecasting. In 2005, Dr. Schaden additionally became Head of the Infineon Corporate Competitive Intelligence Department. The Competitive Intelligence team is responsible for all market, competitor and economy related topics on a corporate level. Dr. Schaden got her Ph. D. degree in Economics at Constance University.

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10:50 am — 11:20 am
Saal 2

Ulrich Schaefer, Bosch

Limits to IC Market Development: Product Development

From the expected development of the total worldwide IC market it will be shown, how the future number of needed IC designers develops during the next 15 years. A comparison with the actual number of engineering students, who are at the universities today, and younger school students, who may choose this profession in the near future, shows that there will be a wide gap between the demand and supply. In addition it seems from past experience that the advance of EDA tools especially for analog and mixed signal ASICs/ASSPs develops significantly slower than needed. Since the continually enhancing demand of manpower on designs can most probably not be fulfilled, the future increase of EDA tool complexity seems crucial for the continuation of the forecasted development of electronics.

This talk deals with the discrepancy between the diverging need of IC designers and the available junior staff, which can only be met by an enhanced development of EDA tools and methods.

Ulrich Schaefer
Automotive Electronics
Robert Bosch GmbH

Dr. Ulrich Schaefer studied physics at the universities of Braunschweig and Bonn until 1981 where he got his Ph.D. graduation in elementary particle physics. From 1981 to 1986 he worked on production planning and control, process development and purchase of equipment for thick film hybrid manufacturing at Blaupunkt in Hildesheim. In 1986 he joined the Robert Bosch GmbH in Reutlingen to work on process development of thick film hybrid manufacturing until 1989 and on design and layout of automotive ECUs, process development of PC-board production from 1989 to 1995. Since 1995 he is responsible for market research in semiconductors and the representation of Bosch at several industry associations e.g. EECA-ESIA, SICAS, WSTS, ZVEI.

Since 2004 he is member of the board of directors of the EECA-ESIA: and from 1999 to 2005 he was European vice chairman of the WSTS of which he became world chairman in 2008. Since 2002 he is also chairman of the semiconductor group in the ZVEI and member of the board of the division ECS (electronic components and systems).

"IT'S MY LIFE" - More (Robust) Chips for no Failures During Lifetime

Session Keynote:

Subhasish Mitra, Stanford University

Globally Optimized Robust System Design

Future system design methodologies must accept the fact that the underlying hardware will be imperfect, and enable design of robust systems that are resilient to such imperfections. This talk will describe enabling tools and technologies for building such systems. This presentation is about three techniques that can enable a sea change in robust system design:

1. Built-In Soft Error Resilience (BISER)
2. Circuit Failure Prediction
3. Concurrent Autonomous Self-Test and Self-Diagnosis

These techniques span multiple abstraction layers (circuit, architecture, virtualization and application), and enable global optimization across these layers. The applicability of robust system design techniques in overcoming the growing challenge of post-Silicon validation will also be discussed.

Subhasish Mitra
Departments of Electrical Engineering and Computer Science
Stanford University

Dr. Subhasish Mitra is an Assistant Professor in the Departments of Electrical Engineering and Computer Science of Stanford University. His research interests include robust system design, VLSI design, CAD and test, and design for emerging nanotechnologies. Prior to joining Stanford, he was a Principal Engineer at Intel. He received Ph.D. in EE from Stanford.
Dr. Mitra has co-authored more than 100 technical papers, and his robust system design techniques have seen wide-spread proliferation. His X-Compact technique for test compression is used by more than 50 Intel products, and is supported by major CAD tools. His work on imperfection-immune circuits using carbon nanotubes, jointly with his students and collaborators, has been highlighted as a "significant breakthrough" by the Semiconductor Research Corporation, MIT Technology Review, EE Times, and many others. His major honours include the NSF CAREER Award, Terman Fellowship, IEEE TCAD and DAC Best Paper Awards, ACM SIGDA Outstanding New Faculty Award, Intel Divisional Recognition Award and the Intel Achievement Award, Intel's highest corporate honour, "for a breakthrough test compression technology."

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9:35 am — 10:20 am
Saal 1

"IT'S MY LIFE" - More (Robust) Chips for no Failures During Lifetime

Alison Burdett, Toumaz Technology

The Sensium™: Designing a Robust and Reliable Ultra-Low Power System-on-Chip for Wireless Medical Monitoring

Medical devices need to achieve very high levels of reliability. Hardware redundancy and software self-test routines are typically employed to guarantee device operation, and extensive testing post-manufacture is needed. As a result, components designed for use in medical devices are significantly more expensive than similar components intended for use in consumer devices.

Toumaz Technology has recently developed the Sensium™; an ultra-low power system-on-chip (SoC) for wireless medical monitoring. This SoC is integrated with appropriate sensors and printed battery to produce a disposable patch – or 'digital plaster' – which can be used to monitor the vital signs of a patient. Since the patch is disposable, low cost is important, but high levels of reliability are still necessary. This talk will discuss how self-test and reliability were inherently designed into the Sensium, to ensure the goals of robust operation and low manufacturing costs could both be achieved.

Alison Burdett
Director of Technology
Toumaz Technology Ltd

Dr. Alison Burdett received the BEng degree in 1989 and Ph.D. in 1992, both from Imperial College, London. After working for GEC-Plessey as an integrated circuit designer, she re-joined the Department of Electrical and Electronic Engineering, Imperial College in 1994 as Senior Lecturer in Analog Circuit Design. In 2001 Dr Burdett left Imperial College to co-found Toumaz Technology Ltd, a fabless semiconductor company involved in ultra low power and RF integrated circuit design. She is currently Director of Technology at Toumaz Technology, and is responsible for technology development within the company, including the implementation of research programmes in conjunction with UK and international universities and industry. Dr Burdett is a Chartered Engineer, a Fellow of the Institute of Engineering and Technology (FIET) and a Senior Member of the Institute of Electrical and Electronic Engineers (SMIEEE). Dr Burdett has published over 70 peer-reviewed technical publications and holds 15 patents.

Friday, Dec. 12, 2008
10:50 am — 11:20 am
Saal 1

A long life without failures is a goal that everybody would like to achieve. Surely we should then think about robustness, how to get it, to keep it and to take advantages of it.

Christoph Heer, Infineon

Future Robust Systems Require Holistic Approaches Combining Hardware and Software Concepts

Continuous cost reduction is essential for successful semiconductor business. Technology scaling supports the reduction of variable product cost, but brings many new challenges with every technology node as chip designers are facing new failure types and even higher failure probabilities. While the application level including software and firmware may further increase the failure probability, it also provides additional means to address them. This is an increasing challenge especially for safety applications like in the automotive industry due to the strict separation of hardware and software development. This presentation will address the fundamental failure mechanisms and propose a paradigm shift in design methodology to address the robustness of future highly complex systems on chips.

Christoph Heer
Senior Director
Infineon Technologies AG

Dr. Christoph Heer, Senior Director at Infineon Technologies, is responsible for "Digital IP and Re-use" of standard components for large scale integrated digital circuits. This includes the definition of the technical roadmaps for future advanced CMOS technologies and the development of a design environment for manufacturing technologies from 180nm down to 65nm. He is also responsible for a global organisation with teams in Sophia Antipolis (France), Bangalore (India) and Munich (Germany).

Dr. Heer received a Diploma degree in solid state electronics from Aachen University of Technology in 1990 and a Ph.D. degree in electrical engineering from Ulm University in 1995. Dr. Heer has published more than 50 papers in peer-reviewed international journals and conferences. He has been member of the technical program committees of various international conferences including DAC, DATE and ASYNC.

Friday, Dec. 12, 2008
11:20 am — 11:50 am
Saal 1

Moderator: Peggy Aycinena, EDA Confidential

More EDA for a Better Future in Microelectronics

As the EDA industry matures, complete with high-profile consolidations and acquisitions, the eternal question remains – should EDA customer companies develop and support their own internal CAD tools, or should they rely on the EDA vendors for those tools? The answer may vary from customer to customer, depending on each customer's internal resources. However the answer may also depend on the customer's view of the quality of the offerings from the EDA vendors, and the willingness of the EDA vendors to work in partnership with their customers to develop and maintain cutting-edge tools. Have recent developments across the business landscape in the EDA industry made the EDA vendors more or less responsive to the needs of their customers? Do the EDA customers believe the availability of more third-party tools will be crucial to their success going forward? This panel of EDA customers will provide their perspective on the EDA industry from a business point of view.

Panellists will be some of the speakers as well as namable persons of the industry.

15 min.: Opening remarks by P. Aycinena, EDA Confidential
30 min.: Q&A – Aycinena with panelists
15 min.: Q&A – Panelists take questions from audience

Peggy Aycinena
Editor
EDA Confidential
Contributing Editor
EDA Weekly

Peggy Aycinena is a journalist based in Silicon Valley, Editor of EDA Confidential, and Contributing Editor to EDA Weekly and the DACeZine. She has served as session chair at DAC and DATE, and is a member of the DAC Exhibitor Liaison Committee. Previously, she served as managing editor of Visual Studio Magazine, staff editor of Chip Design Magazine, contributing editor for in Play in EDA and EDA Nation, and editor of ISD Magazine. Aycinena's articles have appeared in print the Communications of the ACM, ISD Magazine, EETimes, and Intelligent Enterprise. She is published online in EDACafe, DACeZine, FTPonline, TechOnline, Chip Design, SOCcentral, and EEDesign. Aycinena has a B.A. in Biophysics from U.C. Berkeley and a B.S. in Electrical Engineering from San Francisco State University.

Friday, Dec. 12, 2008
11:55 am — 12:55 pm
Saal 1

More Solutions Provided by EDA Vendors

In order to realize the fascinating applications and promising business opportunities discussed in edaForum08´s sessions it is indispensable to have access to professional tools and design flow solutions, completed by professional services. In an exhibition and in short talks within the Company Presentations Session leading EDA vendors will present their tools and solutions for applications and issues like that discussed in edaForum08´s technical and business sessions.

The exhibiting vendors will be asked to present their answers for the problems designers face in their daily work today. This part will be prepared in close cooperation with the active and growing IC-Design Working Group representing almost 700 IC designers within the "Silicon Saxony Technology Network". The EDA vendors will be invited to discuss with companies like AMD, NXP, Qimonda, X-FAB, ZMD and many others appropriate solutions for their design projects and to give an update on their tool offering, however focussing on what is new and is solving burning issues.

Heinz Martin Esser, member of the board will introduce the Silicon Saxony Technology Network and highlight the work of its IC-Design Working Group.

After the Company Presentations all participants will be invited to a sponsored lunch.

Participating companies:

chipvision

OneSpin Solutions

CST

Silicon Saxony

These companies confirmed their participation until the press date of this program. For a recent list please visit:
www.edacentrum.de/cp

Thursday, Dec. 11, 2008
9:00 am — 1:00 pm
Saal 2

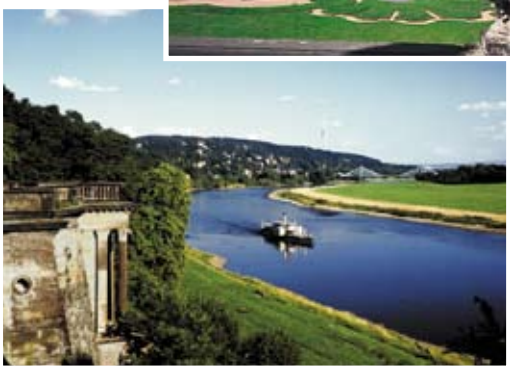
Location

Dresden, the capital of Saxony and the former residence of the Wettin dynasty, is a city of art and culture with magnificent buildings, many world-class museums as well as a rich tradition of theatre and music.

No book about the history of architecture can forget to mention Dresden's Zwinger Palace. The reconstructed Frauenkirche, the Semper Opera House and the Royal Palace as well as many other historical monuments and collections define the image of the city.

Dresden has built up a reputation as a location for semiconductor business, where several companies established new locations. Additionally, with the mask technology center AMTC, the co-operating companies have built the most modern plant of its kind world-wide, which is a model for further investments in nanoelectronics.

In December, visiting the famous "Striezelmarkt", is a must. This is one of the oldest German Christmas fairs, which attracts thousands of visitors every year. A special attraction at the Christmas fair is the 14-meter high Christmas pyramid. This biggest pyramid in the world is decorated with 42 wooden figures.



See also: www.dresden.de

Accommodation

The Hilton Dresden is right in the middle of the historical old town, between the reconstructed Frauenkirche and Brühl's Terrace. The Semper Opera, Dresden Castle with its Green Vault, and the world-famous Zwinger Palace are just a few minutes' walk from the hotel. The Hilton Dresden has 12 restaurants, cafés & bars offering a variety of culinary delights. At the start of the day or to close an eventful day you will regain your equilibrium at the LivingWell Health Club. An area of 1,100 square metre is dedicated exclusively to regenerating body, mind and spirit.

For edaForum attendees edacentrum has arranged the following special room rates, valid during the edaForum08, available only for bookings by fax or phone:

Single room EUR 195 (incl. breakfast)
Double room EUR 220 (incl. breakfast)

Please book your room by October 10, 2008, and mention "edaForum08" as the keyword. After October 10, the fixed quota of rooms for the edaforum08 will be closed. We recommend that you book early as the hotel could be booked up very quickly when trade fairs are taking place.

The hotel booking form is available via www (s. below) and will be sent by e-mail together with the confirmation of registration. All participants are kindly asked to make their own hotel reservations directly:

Hilton Hotel Dresden
An der Frauenkirche 5
01067 Dresden
Germany
Phone: +49 351 8642-0
Fax: +49 351 8642-889

See also: www.dresden.hilton.com

The hotel booking form is available at www.edacentrum.de/edaforum/hotel_reservation.pdf

Directions to Hilton Hotel Dresden

From the north and the east (Berlin, Bautzen) via A13/14
Exit Nr. 81 Dresden Hellerau/ city center. Follow B170/ E55 towards city center/ Prag. At the first traffic light after the "Carolabrücke bridge", turn left twice towards the river Elbe and follow the signs "Hilton Dresden".

From the west (Frankfurt/M, München, Leipzig) via A4/A14
Exit Nr. 78 Dresden "Altstadt" towards Dresden city center/ B6 (approximately 4 km) to the Semper Opera House / river Elbe. Turn right after the second bridge and follow the signs "Hilton Dresden".

From the south (Prag) via A17
E55/ B170 towards city center, at the third traffic light (just before the bridge) turn right towards the river Elbe and follow the signs "Hilton Dresden".

From the main railway station
From Dresden main station take the number 8 tram (direction Dresden Kiefernweg), get off at "Theaterplatz" stop, then walk along "Augustusstraße" towards the Frauenkirche. It takes about 5 minutes.

See also: www.dvbag.de

From the airport

By public transport:
Take S2 local train (direction Pirna Bahnhof). At "Dresden-Neustadt" stop walk about five minutes to "Dresden Bf Neustadt (Hansastr)" stop and take the number 9 tram (direction Dresden Prohlis), get off at "Theaterplatz" stop. Walk along "Augustusstraße" towards the Frauenkirche. It takes about 5 minutes.

By car:
Follow airport road into town towards the city center, straight on all the way, after the "Carolabrücke" bridge turn left twice towards the river Elbe and follow the signs "Hilton Dresden".

By taxi:
The taxi stand is directly in front of the terminal entrance. The taxi fare to the city centre ranges from EUR 16 to EUR 18.

See also: www.dresden-airport.de/en

Registration

Registration:	**until Oct. 31**	**until Nov. 14**
edacentrum members*	**EUR 595**	**EUR 645**
Non-members	**EUR 995**	**EUR 1,045**

(All prices plus 19% VAT)

Late registrations cannot be guaranteed and will be charged an additional fee of EUR 50 (plus 19% VAT).

The edaForum08 participation fee includes company presentations, forum, social event, trips and tours, 2x lunch, conference beverages, conference documents and one free copy of edaTrend DAC08 report. This is an all-inclusive package. Items are not available separately.

Payment is possible by invoice or credit card: MasterCard, VISA or AMEX. (We need to have the "card verification code" for credit card transactions.)

* For information and conditions concerning membership at edacentrum see www.edacentrum.de/membership.html

To register choose the registration online (s. below) or fax the registration form to +49 511 762 19695.

For further request please contact:

edacentrum
Ms. Maren Sperber
Schneiderberg 32
30167 Hannover
Germany

Phone: +49 511 762-19699
E-mail: edaforum@edacentrum.de

Registrations are processed in the order they are received. Confirmation receipts will be sent via e-mail if an e-mail address is provided. Otherwise, confirmation letters are posted within 7 to 10 business days of processing. Please review your registration confirmation for accuracy.

The registration desk at the edaForum08 will be located in front of the conference rooms during edaForum08:
December 11, 8:00 am - 5:30 pm
December 12, 8:15 am - 2:00 pm

Cancellation

Cancellation (only by written request) is possible free of charge until November 21, 2008. Until November 28, 2008, half of the participation fee is retained. After this date the entire participation fee is due. A replacement for the registered participant with the same affiliation is possible at any time.

Frauenkirche (2:30 pm – 4:30 pm)
The Dresden Frauenkirche can look back on a 1000-year history. The churches preceding it were dedicated to "Our Lady" and called Frauenkirche. In the 18th century, the famous dome structure by George Bähr was built and this dominated Dresden's cityscape for 200 years. The church was destroyed shortly before the end of World War II. The ruins remained as a memorial in the heart of the city. The conviction that the Frauenkirche had to be rebuilt was shared by many people. But it took 45 years before fulfilling this dream became a feasible possibility. And, in total, 60 years went by before the Frauenkirche in all its baroque beauty could reopen its doors to the world.

The guided tour of the prayer stalls and the first gallery explains the history of the Frauenkirche, the rebuilding process and the church area, and gives knowledgeable answers to all questions.

See also: www.frauenkirche-dresden.de

Christmas in the Landhaus (2:30 pm – 4:30 pm)
This year's exhibition at the City Museum focuses on the decorated Christmas tree and the festive décor and design of the Christmas celebration from Biedermeier to the present day. It addresses not only the changes that Christmas tree décor has undergone over the centuries, but also the diverse range of Christmas tree decorations available. And the large-scale model train exhibit will also be on hand again.

See also: www.stmd.de

Friday, Dec. 12, 2008
2:30 pm
Meetingpoint at the Hotel reception

Ice skating (2:30 pm – 5:00 pm)
From the first weekend in Advent, "Germany's most beautiful ice rink" will be open in the historical inner courtyard of the Kempinski Hotel Taschenbergpalais. In a romantic baroque atmosphere you can both skate and relax with hot homemade mulled wine and snacks at the snow-bar. Of course ice skates for everybody will be available there.

Deutsches Hygiene-Museum (2:30 pm – 5:00 pm)
Since its creation in 1911, the Deutsches Hygiene-Museum has striven to prevent disease by enlightening the public. The museum has always portrayed the body in a gamut of contexts, ranging from the individual threatened by illnesses to a frequently idealized notion of health. Since 1930, the "Transparent Man" has served as the symbol of this museum. This figure depicts the internal workings of the human body as a machine: understandable, immaculate, and, if well cared for, durable In another exhibition you may learn about the cosmos of the human brain: How does our brain work and what does it do? Furthermore the exhibition "2° Weather, Climate, Man" combines media installations and interactive elements with objects from natural history and cultural history, art and science in an exciting learning experience. One of these three topics, the "Transparent Man", the cosmos of the human brain or the "2° Weather, Climate, Man" will be explained in a guided tour.

See also: www.dhmd.de

Friday, Dec. 12, 2008
2:30 pm
Meetingpoint at the Hotel reception

Baroque Dinner

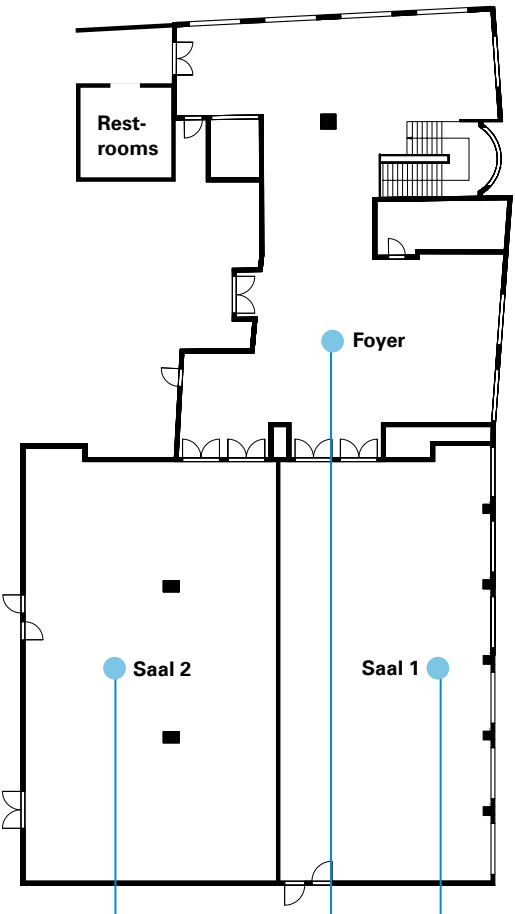
Follow our invitation to a very special culinary and musical evening in baroque surroundings. A delightful menu is waiting for you in the beautiful Salon Europa of the historical Prinzenpalais building. Rejoice in the panoramic view of the river Elbe on the terrace of the Prinzenpalais and enjoy a communicative event accompanied by a musical journey through time.

Our Venezia Sextet chamber orchestra starts its musical journey with famous classical tunes followed by novel interpretations of baroque music. In conjunction with glorious baroque costumes this will be a pleasure for the eye and the ear. Finally the ensemble will finish the journey through time with selected music from modern times.

Furthermore there will be the presentation of the EDA Achievement Award during the social event. The award is conferred by the edacentrum to award special research or development efforts in the area of EDA in Germany; especially efforts which have been funded by the German BMBF-funding program Ekompass.

Thursday, Dec. 11, 2008
7:00 pm
Salon Europa, Hilton Hotel

Floor Plan of Hilton Hotel Dresden



Saal 2
Business Session
Company Presentation

Foyer
Registration
EDA Lounge
Coffee Break

Saal 1
Technical Session
General Keynote
Friday Keynote
Panel Discussion

The edaForum is organized by

edacentrum

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About the past events

With the first six edaForum events (Hannover 2002 and 2005, Stuttgart 2003, Dresden 2004, Berlin 2006, München 2007), edacentrum established a unique event for decision makers. The feedback from attendees emphasizes the outstanding networking opportunities, the top class speakers and the special focus:

Hermann Eul, Infineon Technologies AG:
„edaForum07 was an exciting place to go: good talks, interesting people, valuable information and a lot of networking, in short: a very recommendable event - very important for the industry."

Aldo Romano, STMicroelectronics Italy:
"What I liked most at the edaForum06 was the perfect organization and the value of participants: I found very stimulating the possibility of meeting in the same environment important customers, valuable competitors and the best software suppliers. Excellent organization in an impressive city."

Alberto Sangiovanni-Vincentelli,
University of California at Berkeley:
"It was a real pleasure to participate to edaForum05 as I had an opportunity for interaction with key people in our industry in a vibrant environment. I particularly appreciated the mix of technical and business content that the workshop offers; a combination that is hard to find in existing conferences and workshops."

Tom DeMarco, Principal of The Atlantic Systems Guild:
"The 2004 edaForum was the first I've attended, and I came away very impressed. The quality of the networking at this event was unmatched. The interaction among attendees was frank and extremely useful. Of the many conferences I regularly attend, I can't think of any which surpasses edaForum in establishing an active and sharing community of interest."