The edacentrum e.V. is an independent association dedicated to the promotion of research and development in the area of electronic design automation (EDA). Its main role is to initiate, evaluate and supervise EDA R&D projects. Further by encouraging basic research projects and EDA networks, it bundles and reinforces the EDA expertise of the German research community. The edacentrum actively engages in public relations in order to sensitize higher management levels, the public and the political arena about the central importance of design automation in microelectronics.

The association helps identify and define research projects on national and international level. In particular, it assists in the preparation and implementation of national and international EDA R&D projects funded by public authorities.

The edacentrum pursues the following strategic goals. It coordinates research and suggests new research topics, channels expertise into effective action and creates new and innovative networks; motivates and consults companies and research institutes in their use of new design methods; secures the processing and steady use of new design tools by assisting in EDA software commercialization; strengthens the market through international cooperation and standardization; supports the BMBF (German Ministry of Education and Research) with its expertise. At present, 45 companies are member of the edacentrum. As an association, the edacentrum e.V. is open to all persons and legal entities.

Directions to the Hilton Hotel Dresden, Conference location and accommodation (the Hotel is situated opposite to the “Frauenkirche”)

Arrival by train:
From central station take …
… a taxi/taxi (approximately 10 minutes)
… the tram No. 8 (to “Hellerau”), get off at stop “Theaterplatz.”
Walk along the “Augustusstraße” towards “Frauenkirche”
(5 min walk)
www.bahn.de
www.efa.de
www.dvb.de

Arrival by car
From the north via the A4 motorway:
Leave motorway exit “Dresden-Hellerau”, then follow the signs to the city center (“Zentrum”) on the Hotel Route B (red)

From the west/south via the A4 motorway:
Exit motorway exit „Dresden-Altstadt“ then follow the signs to the city center (“Zentrum”) on the Hotel Route D, change to Hotel Route A at “Nossener Brücke”

www.stadtplan.net
www.stadtplandienst.de

Arrival by plane:
From airport Dresden (DRS) take …
… a taxi/cab (approximately 30 minutes)
… the train and train
Link S2 (to s-xl station), change at “Bahnhof Neustadt” into train No. 3 (to “Coschütz”). Get off at stop “Synagoge.” Walk along “Trscherplatz/ Pöpernstraße” towards “Frauenkirche”
(5 min walk)
… a rental car
From the airport via A4 leave motorway exit „Dresden-Altstadt“
and proceed as written above.

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Preface

This year Ron Collett, well known President and CEO of Numetrics Management Systems Inc., wrote for the Fabless Forum: “85% of IC projects (ASIC and ASSP) miss their target schedule. The average overrun is 53%. A primary reason for schedule misses is due to under-estimating the complexity of the design and over-estimating the productivity of the development team.” Are you among the lucky 15% that have never faced this problem (if they exist at all!)? Or do you believe like me, that complexity and productivity are amongst the most important challenges for success in microelectronics? If so, you should seriously consider to attend edaForum04!

In 2004 edaForum goes into its third year and it has developed into a remarkable and unique event. Its objective is to bring together decision makers from industry and top-rated speakers from all over the world. With its dual focus on technical issues and business aspects it has established a new culture of discussion within and about Electronic Design Automation (EDA). EDA is the key to mastering complexity and to drive productivity.

This year we have set a special priority on meeting project schedules. We have invited Tom DeMarco, author of numerous publications on project management, to give us a more general view, enabling us to learn from experience in other industries. We have organized two business sessions focussing on Design and Productivity, Design on Time and Budget, and two technical sessions reviewing Design for Manufacturing and Yield as well as Design for Verification and Test. Discuss with us the challenges of chip design and EDA. We provide you with pleasant opportunities not only to listen to invited talks given by true experts but also to discuss your problems and views. Visit the EDA Lounge, relax during our special social evening event and join one of the excursions. And if you still hesitate: Dresden is a beautiful place to go with so many more possibilities to spend a weekend, when edaForum04 closes.

On behalf of the edacentrum I cordially invite you to the third edaForum.

Erich Barke
Chairman edacentrum
Project work is a risky business. Avoiding risk is a no-win proposition because risk is usually an indicator of value; when there is no risk there is no value. We need to learn to run toward risk, not run away from it. (If a project has no risks at all, don’t do it!). But when you’re running toward risk you also need to take certain reasonable precautions. These precautions make up the heart of the discipline called risk management.

Companies that don’t manage their risks reasonably can only afford to take small risks. That presents a paradox: risk management is not so much a way to banish risks as it is an enabler for aggressive risk taking. The companies that will succeed in today’s frenetic business climate are the ones that can confidently take the biggest risks. Their confidence is not the same as foolhardiness: they don’t count on never being beaten by a risk. What they count on is winning big when they win and losing small when they lose.

The distinction between confidence and foolhardiness is key. Managers for years have been taught to instill a “Can Do” attitude in themselves and everyone who works for them. When Can Do is the rule, any concentration on the possible project pitfalls is frowned upon. Everyone is expected to think positive and not get all bothered over things that might go wrong. Running a Can Do operation is often portrayed as hard nosed management, but it’s really more like kid stuff. It sets a date for completion and then refuses to consider any other alternative. Can Do is another term for foolhardy management.

A short list of the skills of risk management would include the following: risk assessment, risk discovery brainstorming, exposure analysis, uncertainty diagramming, contingency planning, risk mitigation, Monte Carlo simulation, handling of unmanaged risks, incremental implementation, Earned Value Running (EVR) metrics, mastery of the five core project risks.

In this 60-minute presentation, Tom DeMarco lays out the how-to’s of risk management and makes the case for including this new discipline in your organization.
Tom DeMarco is a Principal of the Atlantic Systems Guild, a systems think tank with offices in the U.S., Germany and Great Britain. His consulting activity focuses on project management and litigation involving software intensive endeavors.

He is a past winner of the Jean-Dominique Warnier Prize for “lifetime contribution to the information sciences.” He is a founder and past-president of the PspTech Conference and a Fellow of the Cutter Consortium.

DeMarco is the author of nine books on management, organizational design, and systems development. The most recent is called “Waltzing With Bears: Managing Risk on Software Projects,” written with co-author Tim Lister. (If you think waltzing with a bear is risky, try managing a software project.) Before that there was “Slack: Getting Past Burnout, Busywork, and the Myth of Total Efficiency,” published by Random House, Broadway Books Division, in 2002. It addresses the question, Why are we all so damned busy? and offers some unsettling answers. In 1997, he wrote “The Deadline: A Novel About Project Management” published by Dorset House Press, the story of a veteran software manager who finds he has bet his life on a project deadline. The book is about managing as though your life were on the line.

DeMarco’s career began at Bell Telephone Laboratories where he served as part of the now-legendary ESS-1 project. In later years, he managed real-time projects for La CEGOS Informatic in France, and was responsible for distributed on-line banking systems installed in Sweden, Holland, France and Finland. He has lectured and consulted throughout the Americas, Europe, Africa, Australia and the Far East.

DeMarco has a BSEE degree from Cornell University, an M.S. from Columbia University, a diploma from the University of Paris at the Sorbonne, plus an honorary Doctor of Science from City University London (2003). In 1999 he was elected a Fellow of the IEEE. He is the winner of the 1999 Stevens Award for his contribution to software engineering methods. His first work of mainstream fiction, a comic novel called Dark Harbor House, was published by Down East Books in the Spring of 2001. His short story collection, Lieutenant America and Miss Apple Pie was published in 2003. He makes his home in Camden, Maine.
ANOTHER BRICK IN THE WALL
Design for Manufacturing and Yield

Keynote

Manufacturability Profiling of IC Designs: Obvious and not so Obvious Manufacturability Design Attributes

Manufacturability of an IC is a notion which seems to be well understood. It is usually characterized in terms of predicted yield loss for a given design. But in reality, yield predictions are feasible only for a fraction of phenomena which cause IC failures. Also yield loss is not a number – it is a function of time. As a result, IC designers as well as CAD tools use “intuitive manufacturability indicators” instead of yield estimates. For example these include pattern density, number of vias and few other similar figures to guide design and CAD tools. The purpose of this talk is to analyze whether these “manufacturability indicators” are sufficient to achieve producible designs. Additionally in this talk a research agenda will be formulated, which will enhance the currently used portfolio of manufacturability indicators.

Wojciech Maly received the Ph.D. degree from the Institute of Applied Cybernetics, Polish Academy of Sciences, in 1975. In 1975, he was appointed Assistant Professor at the Technical University of Warsaw. From September 1979 to July 1981, he was a Visiting Assistant Professor of Electrical and Computer Engineering at Carnegie Mellon University, where he has become the Whitaker Professor of Electrical and Computer Engineering.

Dr. Maly’s research interests have been focused on the interfaces between VLSI design, testing and manufacturing with the stress on the stochastic nature of phenomena relating these three VLSI domains. He has authored, co-authored and edited a number of books, journal and conference papers as well as patents, promoting the integration of design, test and manufacturing.

Dr. Maly was elected an IEEE Fellow in 1990 and has been recipient or co-recipient of various awards including honors for his Ph.D. thesis and the Eta Kappa Nu CMU Sigma Chapter Excellence in Teaching Award.

December 9th, 2004
02.30 pm - 03.15 pm
Room: Rotterdam
As the nanometer era is approaching, the red brick wall is coming closer too. Is Design for Manufacturing and Yield a method to remove another brick from that wall?

Nanometer-Era Design for Manufacturability

In the nanometer era, the spectrum of physical phenomena that can contribute to significant yield losses is mind-boggling. The most accurate way of accounting for these effects is to provide accurate physical models and then simulate the actual IC layout to estimate the impact on yield and performance. Such a simulator must be calibrated to the actual manufacturing process by specially designed test structures that cover all possible layout patterns found in real products. A set of Characterization Vehicles (CV™) that are used for extraction of defectivity, fail rates and performance variability characteristics of a given fabrication process will be presented. This modeling-based approach can be then used for generation of “guaranteed to yield” IP blocks and can also serve as a yield sign-off tool for the entire IC layout. Examples of the improved set of IPs and silicon verification results demonstrating the yield gain will be shown. Then a rigorous decision tree based approach to the root cause analysis and fixing of the top yield detractors will be introduced, followed by a comprehensive set of product engineering solutions. Finally the talk covers the actual yield learning results obtained by employing this comprehensive methodology to the process and product ramps for several lead products in the most advanced technology nodes.

Andrzej J. Strojwas has served as a technical advisor to PDF since the company was launched and was appointed PDF’s Chief Technologist in 1997. Currently the Keithley Professor of Electrical and Computer Engineering at Carnegie Mellon University, Dr. Strojwas’ career spans over 25 years as an expert in the electronics manufacturing industry. He has held senior technical positions at Harris Semiconductor Co., AT&T Bell Laboratories, Texas Instruments, NEC, Hitachi, SEMATECH and KLA-Tencor, and has consulted for several semiconductor companies, equipment vendors and EDA companies in the area of statistically based CAD/CIM of VLSI circuits. Dr. Strojwas is an IEEE Fellow.
Yield as Fourth Design Target, the Challenge of Design for Yield

In the area of UDSM and today’s continuously changing market conditions, yield ramp has become a key factor in driving product profitability. While product complexity is increasing the market windows are shrinking, a delay means decreased revenue as prices decline.

Painful ramping at the 130 nm node taught the industry a few important lessons:

» Productivity advances in the future will come not only by feature shrinks, but also by new materials.
» Yield ramping and final yields will not reach historical norms.
» A key cause of not reaching previously attained yield levels is the gap between design and manufacturing.

For critical device features < 0.25 µm the separation between design and manufacturing was not the main issue. Today as the industry is ramping 90 nm and developing 65 nm the design rules have become inadequate to describe the manufacturing reality and its impact on the design process. Also, the process variations definitely start becoming a nightmare for 65 and 45 nm devices.

As consequence of driving product profitability, yield as quality factor must be included as target besides area, performance and leakage during all stages of the design process. It turns out that a big time saving factor during ramp of a product is the early communication of design areas, that may be marginal in terms of design rules, defect density sensitivity etc., where metrology or inspections could focus on.

In the first part of the talk we address the need of introducing yield as fourth design target and its consequences for EDA tools. In the second part we concentrate on a proper Design for Yield & Manufacturability interface between the design and the manufacturing phase.

December 9th, 2004
04.15 pm - 04.45 pm
Room: Rotterdam
Bernd Lemaitre received the Diploma degree in Physics from Technical University Darmstadt, Germany and the Institute of Nuclear Physics and the PhD in Electronics from the University of Bundeswehr, Munich in 1992. In 1985 he joined Siemens AG, Semiconductor Division, now Infineon Technologies AG. As leader of a simulation group with the main interest in device modeling for enhanced CMOS technologies he worked in the area of CAD, technology development, device modeling and characterization. From 1998 to 2002 he held the position of a Vice Chairman of the international Compact Model Council organized by the Electronic Industries Association (EIA). Since 2002 he is working in the area of Yield Management and Design for Manufacturing as a program manager for DfM at Infineon Technologies AG.

Uwe Gäbler received the Diploma degree in Electrical Engineering from Technical University Dresden, Germany in 1992. In 1992 he joined Fraunhofer Gesellschaft, Institute of Microelectronic Circuits and Systems Duisburg/Dresden, now IPMS Dresden. He worked in the area of circuit design, especially for digital and mixed-signal ASICs. From 1997 to 2001 he was working at Siemens HL, now Infineon, in the Product Engineering Department as Lead Engineer for quarter micron logic technology. From 2001 to 2003 he was working in the area of Design for Manufacturing, especially responsible for interaction between development and fabs. Since 2003 he is project leader of an Infineon project to speed up yield learning for sub-quarter micron technologies.
Each year semiconductor and electronics companies collectively spend billions of dollars on chip development projects that end up getting cancelled. For the most part, the R&D is wasted, because only a fraction of the scrap typically can be leveraged into other projects. It goes without saying that there’s an enormous and direct impact on each company’s financial bottom line. What’s more, these projects chew up precious resources that could be allocated to other projects, which themselves end up missing schedule because they’re inadequately staffed. Late market entry translates into billions of dollars in lost market share annually among competitors. Indeed, the semiconductor industry misses its product development schedules 85 percent of the time, with the average overrun exceeding 50 percent of the originally planned cycle time. Much of this waste can be avoided by applying best practices at both the portfolio and project level, across the full IC development lifecycle—i.e. from project inception through release to volume production. But what are these portfolio and lifecycle management practices and how are they applied?

On the one hand, the practices seem obvious because it’s easy to understand why projects are cancelled and miss schedules so badly. It’s the “usual suspects,” such as instability of manufacturing process and libraries, EDA tool and methodology problems, ill-defined and continuously changing specifications, development team inexperience and/or lack of cohesiveness, IP whose delivery is delayed or doesn’t work as planned, unanticipated technical problems in hardware and/or software, and the premature departure of key resources from the project. Managers know these all too well. But the problem they face is the uncertainty regarding which ones will occur on any particular project and the specific impact of each on schedule. What’s missing is an easy, yet reliable, approach for accurately quantifying the aggregate risk associated with each project and an efficient process that effectively mitigates it.

In developing its unique solution, Numetrics benchmarked and studied over a thousand IC development projects from over 50 semiconductor and electronics companies. This talk delves into the rapidly emerging portfolio and lifecycle management practices that are positively impacting the financial bottom line of semiconductor companies and electronics companies involved in IC development.
Economic survival depends on time to market. Would you like to warp the time to reach the window of success?

Ronald Collett, President and CEO, of Numetrics Management Systems, Inc., has spent nearly 25 years in the electronics industry, where he has held positions in executive management, engineering, marketing and sales. He founded Collett International, Inc. in 1992, a research and consulting company specializing in design technology strategy for semiconductor and electronic design automation (EDA) companies. He also spent several years at the Dataquest division of the Gartner Group, a technology research and consulting firm, where he oversaw the firm’s activities in the areas EDA, application-specific integrated circuits (ASICs) and field programmable gate arrays (FPGAs).

He has published over 100 articles on the design of integrated circuits (ICs) and electronic systems in publications including Electronic Engineering Times, Nikkei Asia Electronics, Nikkei Electronics, Nikkei Micro Devices, Electronic System Design and, most recently, Fabless Forum.

Mr. Collett holds a Bachelor of Science degree in electrical engineering from Drexel University, a degree in law from Santa Clara University, and he is member of the California Bar.
From Home-Made to Tailor-Made: R&D Support for Sourcing Bluetooth Silicon Components

Sourcing departments often are confronted with the task to make rather complex components available within the product design process. Bluetooth baseband components are an interesting example of such a component since they not only constitute a major cost point in the product’s bill of material but also come with a rather complex set of requirements: Regulatory approval of the component, hardware characteristics like size, pinout, number of external components, RF performance and mechanical dimensions are probably already obvious areas of interest that sourcing departments have to deal with ordinarily. For Bluetooth, we also have to consider a substantial amount of software embedded inside the component that has to be evaluated and studied. Highly automated software verification systems play a significant role in this evaluation. The sourcing project also includes some experience of migration from such components already being developed in-house. The presentation will outline the project concept, its main obstacles and lessons learnt. It will not elaborate on the technology details but instead give an overview about the complexity of such sourcing project, its runtime and volume.

Martin Botteck works as a Research Manager in the Nokia Research Center where he leads the Validation and Testing Technologies group since August 1, 2004. Born in 1962, he got his diploma in electrical engineering from the University of Dortmund in 1988, and was awarded a PhD of electrical engineering from the same university in 1993. Dr. Botteck joined the Digital Broadcasting Division of Nokia GmbH in 1993 as a Development Engineer and has since gained experience in various business units such as Consumer Electronics, Nokia Ventures Organization, Mobile Phones and Technology Platforms. In these units he obtained diverse R&D management functions dealing with process and quality issues, Bluetooth application platforms and the d-box decoder project. Since the end of 2001 Dr. Botteck has worked as a Chief Architect for Bluetooth component software and has represented Nokia in standardization and transnational cooperation projects.
Model Based Improvement of Development Processes

Today’s cars are mechatronic systems with high complexity. Up to 70 microcontrollers are used and connected by local networks in a car. The trend to increase functionality (and thus complexity) is ongoing. It is accepted that up to 80 % of future innovation is driven by software, which imposes additional requirements from the customer perspective on safety, reliability and quality, all together on a high level. Moreover, managing costs for providing the increased functionality with the increased requirements is an omnipresent topic. An important and central approach to master this business challenge is the focus on the development processes, which have to be mastered and optimized in a permanent activity. In the mid nineties Bosch started to work with model based process improvement in the domain of software development. Reports in the software community lead to the hope, that following this approach would enable meeting the business challenges mentioned above.

This presentation describes the Capability Maturity Model Integrated (CMMI) with respect to the components of the model, the maturity levels and assessment methods and mastering process improvement. It has been found in practice, that model based improvement is capable of providing a direction for improvement activities and connects to business goals. The effectiveness of process improvement was measured on the basis of improvement in these goals. Subsequent to the success in adopting CMMI for software development, a few business lines are adopting CMMI to other domains like electronic engineering and ASIC development. The final part of this presentation gives an outline about fitting and interpreting CMMI in these domains and focusing towards systems.

Willy Reiss is a department leader at the Corporate Research and Development of BOSCH. He has extensive experience in model based software development, process improvement and development infrastructure supporting business goals. He was born in 1957 and has studied electronic engineering at the University of Stuttgart. He joined Bosch in 1987.

Willy Reiss
Manager,
Transfer Services for Software Intensive Systems,
Corporate R&D, Robert Bosch GmbH

December 9th, 2004
04.15 pm - 04.45 pm
Room: St. Petersburg
Design for Testability: The Path to Deep Submicron

Design has never been simple, but at 130 nm and below – and definitely at 90 nm – it is becoming increasingly difficult. Process and lithography issues continue to drive our advance to new technology nodes. Due to the effects of scaling, defect mechanisms are no longer easily identified with single “stuck at” fault models but rather are demanding far more complex and challenging solutions. For example, shorts are now being extracted from the physical layout of a design, with special tests being created to detect them. But this is just the beginning; delay testing of all transition faults is now a new objective of Design for Testability (DfT). New demands are being made on design to not only create the correct function and help with testing but also to help yield ramp-up. Manufacturing and test are beginning to develop an even stronger relationship due to the close interconnection between yield ramp-up and diagnostics, which are supported by DfT structures included in the design.

In this presentation, T.W. Williams addresses these current challenges. In addition, he will discuss the future challenges facing designers, and the new tools and methodologies which the design community will be dealing with.

Tom W. Williams is a Synopsys Fellow at Synopsys in Boulder, Colorado, U.S.A. Formerly, Dr. Williams was with IBM Microelectronics Division and served as manager of their VLSI Design for Testability group. He received an M.A. in pure mathematics and a Ph.D. in electrical engineering. He has received numerous best paper awards from the IEEE and ACM. He was twice a Distinguished Visitor Lecturer for the IEEE Computer Society. Dr. Williams has previously served on the Computer Society Board of Governors and the IEEE Board of Directors. He is a member of the Eta Kappa Nu, Tau Beta Pi, IEEE, ACM, Sigma Xi, and Phi Kappa Phi. In 1985 and 1997, he was a Guest Professor and Robert Bosch Fellow at the University of Hannover in Germany. Dr. Williams was named an IEEE Fellow in 1988 and received the Computer Society’s W. Wallace McDowell Award for outstanding contributions to the computer art in 1989.

Tom W. Williams
Synopsys Fellow and Director of R&D, Test Development
Synopsys Inc.

December 10th, 2004
09.00 am - 09.45 am
Room: Rotterdam
The last few years have dramatically improved technologies like functional coverage, formal verification, semi-formal methods and assertion-based verification. While the emergence of break-through EDA tools is crucial to keep pace with design complexities, the real challenge for large industrial projects is the successful deployment of these technologies into an evolving design and verification methodology. Design teams are tired of trying out new buzzword technology every year, especially if these just add new workload on top of existing tasks.

The verification methodology for IBM microprocessor and systems development (PowerPC, Cell, G5, p-Series, z-Series) has to scale from functional units to chips containing large systems. A critical part of maintaining a leading-edge verification flow is the ability to systematically improve and adapt it without breaking successful existing technology and practices. The latest evolutionary step for the IBM verification methodology was to embrace the assertion-based verification driven by designers. This extension will be used as a case study to demonstrate principles of how to drive positive technology change into an existing, successful design and verification community.

Wolfgang Roesner got his PhD in electrical engineering at the University of Kaiserslautern, Germany, before he joined the IBM development lab in Böblingen in 1984. There he developed simulators and hardware design languages, later joining the POWER processor development team, where he co-developed the Texsim cycle-based simulation system. His verification tools have been used on all IBM CMOS microprocessor projects, and since 1996 he has been responsible for the overall strategy of verification tools development. Since 2003 he is responsible for IBM Systems Group’s verification methodology and is server verification lead.
Listening to some industry experts, the bar for formal verification has been raised to the point where success is measured by the time it takes for formal methods to replace the more traditional simulation based verification. This is not a helpful stance for the industry or academia. Formal methods are a good complement, but not a replacement technology, whose adoption will be tempered by both technical and economic considerations. Instead of pushing the mathematical basis of a tool, we must concentrate on such issues as: how does it increase an engineer’s productivity? How will it reduce the overall verification time and expense? And how will it ensure that the important bugs have been eradicated? In this presentation both the economic and technical aspects will be explored with one possible outcome being presented.

Brian Bailey is the chief technologist for the Design Verification and Test Division of Mentor Graphics. In this role, Bailey is responsible for setting the technology direction for the group. Previously, Bailey was involved in the creation of the Mentor Graphics Seamless Co-Verification Environment for hardware and software co-simulation. Prior to his work with the Seamless product, Bailey worked with a variety of simulation technologies, including simulation acceleration, emulation, mixed-signal and multi-level simulators. Bailey began his career in the aircraft design business before leaving to work on the emergence of RTL simulation. Bailey graduated from Brunel University in England in 1981 with first class honors in Electrical and Electronic Engineering. He is the Chair of the Accelera Interfaces technical committee and has been active in a number of other standards bodies. He has two patents issued and a number of others pending.
Revolutionary Solutions for Manufacturing Test Required

This talk refers to the economic constraints as they occur in manufacturing of microelectronic systems. Especially the situation for the mandatory manufacturing test will be explained. This leads to the structure of the test flow as it follows the essential steps of creating integrated circuits. Examples from wire line and wireless communication chips are taken to illustrate the semiconductor industry’s current state of the art in testing. The overall test cost of a microelectronic system is structured into the effort for test development as well as the product characterization and operation of volume testing. Both test applications are affected by so called test partitioning which will be described in more detail. Most recent developments in test equipment industry which require more and more EDA support and preferably encapsulation into the design flow will be commented. Even more emphasis is put on EDA contribution if it comes to revolutionary new Design for Test (DfT) approaches targeting the chip level as well as the intermediate hardware between test equipment and the device under test. The so called load board is a challenging key object in cost effective test solutions which may drive given EDA tools and development methodology to its limits. Hot topics in the current ITRS update process and their interaction with other disciplines like package technology will be explained. New EDA solutions have to enable seamless product development and manufacturing flows which manifest in automatic diagnosis of test results. An outline of such leading edge tool flow will conclude the talk.

Peter Muhmenthaler received a Diploma in electrical engineering from the University of Hannover, Germany, in 1988. Since 1989 he is with Infineon Technologies, the former Siemens Semiconductors. Starting with test engineering for DRAMs he moved to design flow development in 1991 with a special focus on macro cell and IP development. In 1995 he built up the center of competence for VLSI test methodology and design for testability. Since 2002 he is director test solutions in the corporate test technology organization.
Globalization is the process of connecting the world’s people with respect to cultural, economical, political, theological and environmental aspects of their lives and creates a web of financial, social, economical and cultural interdependencies. Globalization in business is becoming pervasive and is at the heart of competitiveness of enterprises. Within the high technology sector, the key drivers of globalization are access to key talent and access to new markets. A key focus for this is in the emerging regions of India, Greater China and Eastern Europe including Russia.

This talk will speak to some of the challenges of globalization and lessons learnt in building and effectively managing a global organization across these regions and will propose frameworks for approaching the globalization process in a manner that maximizes success.

Jaswinder Ahuja is the Corporate Vice President and Managing Director of Cadence in India. His responsibilities include the globalization strategy and leading Cadence’s India and Russia Operations. Jaswinder Ahuja started his career with Cadence in 1988 as a software engineer and has led the India operations since 1996. Under his leadership the India center has grown from an R&D site of around 120 to a corporate resource center of over 500 employees. He has led the India center to be recognized for its operational excellence and as the Number One IT Employer in India in 2003 based on the DQ-IDC survey.
Isn’t it all about money? But it need not always be funny, if you search for profitable design procedures.

Venture Capital in EDA

The venture capital industry developed a strong interest for the EDA industry in the late 1990s and went onto an investment spree, which resulted in an over-funding of the industry and in most cases did not yield the anticipated returns. With the years of “irrational exuberance” supposedly behind us, what is the current stand of the venture capital community on EDA?

More specifically, what were the key drivers that led the venture industry to pour substantial amounts of capital in the EDA industry in the first place? What has happened since then and how has the view of the venture community regarding the EDA industry changed? What are venture capital investors now looking for in an EDA investment opportunity? What is the rationale for the venture backing of EDA start-ups in Europe? This talk will try to answer these questions from a venture capitalist’s point of view.

Edouard Lamy is a member of Apax Partners’ IT team, specialising in venture deals. Before joining Apax Partners in August 2003, he worked for three years in the London office of Crescendo Ventures, a global venture capital firm headquartered in California and concentrating on early stage investments in information technology companies. He previously worked as a business development manager at World Telecom labs, a Brussels-based communications technology company, developing advanced carrier switching equipment solutions. Prior to that, he spent two years as an investment analyst in New York at SG Capital Partners. Edouard graduated from Ecole Superieure de Commerce de Paris in 1997.
Sometimes the Answer is Outside the Box

The market and technical pressures of IC design today are forcing engineers away from ASIC-based projects, and forcing them to consider other logic alternatives. ASIC design times are longer than ever experienced, particularly when targeting silicon below 100 nm technology densities. More complex timing prediction, expensive parasitic extraction and analysis tools, new tool training, exorbitant mask costs, and the time and cost of verification in sub-micron ASIC designs now dominate the design flow. But there is a clear alternative available to let you avoid all of this confusion and cost, increase your productivity and at the same time reduce your risk, it is FPGA programmable logic design.

Programmable FPGA-based design methodologies let you increase productivity and lower design costs by removing the silicon design and verification headaches; moving your design freeze much farther out, even after product delivery. FPGA design tools offer added performance advantages with mature tool flows that help ASIC-to-FPGA design conversion with analysis, formal verification, and real-time debug technology that can slash up to 50% off your verification cycle. Advanced optional technology like RT-level floorplanning, FPGA physical synthesis, incremental design, and modular design tailor FPGA implementation tools to your specific corporate design environment, increase design performance, and shorten the design cycle, particularly for high-density designs.

Giles Peckham has worked on the silicon side of IC design for over twenty years, covering the whole spectrum from full custom SoC designs through Standard Cells, Gate Arrays and now Programmable Logic. He currently works for Xilinx where he is responsible for marketing Xilinx’ product and services solutions in Europe. His experience in design and field applications roles supports his special interest in the advanced EDA flows used for today’s high density and high performance FPGAs.

Giles Peckham
European Marketing Manager
Xilinx, Inc.
This talk will examine methods that an ASIC design flow can use to help reduce the full cost of implementing differentiated logic design, also to maintain the competitive advantage of ASICs vs. FPGAs or Structured ASICs.

Cost management is one of the most important implementation considerations for any design manager. While NRE (non-recoverable expenses such as mask costs) and prototype turn-around time are certainly easy to identify and do represent a significant investment for any design team, other significant cost considerations also include the cost of design/characterization, personnel for the duration of the project and the cost of lost opportunity. All of them can grow considerably if the project takes longer than expected to get to market because more than one tape-out is required before the design is stable.

Techniques used by IBM are discussed such as design to maximize yield and design to optimize performance while minimizing power consumption. This is achieved with an ASIC design flow that is fully integrated across all aspects of the semiconductor process and aimed at getting complex, leading edge designs done right the first time.

Jürgen Hilsberg is IBM Technology Group’s European Engineering Manager, based at regional Sales & Marketing headquarters in Geneva. He manages the group’s Field Applications and Field Design Center teams, delivering technical support, including design execution, to IBM Microelectronics’ European customers. They cover the division’s entire product portfolio, including ASICs, embedded IBM PowerPC and Network Processors, integrated set-top box controllers, CMOS & SiGe foundry technologies/services and others. He has almost 15 years of electronics industry experience, primarily in the ASIC and SoC domain. He graduated from the Fachhochschule in Heilbronn, Germany, in 1990, with a degree in electronic engineering.
EDA Tools and Methodologies: A Synopsys Perspective

Design has never been simple, but at 130 nm and below – and definitely at 90 nm – it is becoming increasingly difficult, so much so that design has truly entered a new age. Compute power, multi-media, graphics and communications features are converging in consumer products, putting additional pressure on engineers to create designs that are especially sensitive to cost, power consumption and size. What tools will designers need to successfully face these challenges, and where will those tools come from?

Today, Synopsys is the leading provider of EDA software and services used to design and verify complex ICs, FPGAs and SoCs for the global semiconductor and electronics industries. They provide system-level to silicon-level verification, a complete front-to-back design and test environment, design reuse technology, and professional services to help their customers get their silicon working quickly and accurately. Synopsys solutions include pre-designed and pre-verified blocks of intellectual property (IP) that can be easily inserted into design flows, as well as technology to address yield and manufacturing issues early in the design process.

In this presentation, T. W. Williams addresses these current challenges and future possibilities facing designers, and discusses the tools and methodologies with which Synopsys is responding.

Presenter:
Tom W. Williams
Synopsys Fellow and Director of R&D, Test Development, Synopsys Inc.

Cadence Design Systems, Inc.

The Custom IC Design Challenge

The integration of voice, data, and video, driven by wireless consumer applications, is increasing the IC complexity and the need for analog/mixed-signal and RF content in SoCs. Process technologies are changing fast to ever smaller process nodes. As a result designers are facing several new issues that need to be addressed. Productivity, IP reuse, parasitic closure and yield problems are amongst others the most important ones.

For the successful development of complex ICs a global platform based development approach is essential. The Virtuoso®
Platform and its supported design flows enable a „meet-in-the-middle“ methodology that combines the speed of top-down design with the silicon accuracy of bottom-up design for fast, silicon-accurate analog, custom digital, RF, and mixed-signal design.

Presenter:
Jürgen Hartung
Platform Marketing Manager, Custom IC business unit, Cadence Design Systems, Inc.

Mentor Graphics Corp.

Considerations, Metrics and Measurements for Investment in EDA Tools
EDA has evolved through a series of stages that have each brought new levels of productivity and challenges to the designer. SoC design has typically enjoyed much of the limelight as it pushes the design envelope with each shrinking semiconductor node. However, things have changed now in the worlds of FPGA and PCB design. FPGA fabrics are now being used to characterize some of the world’s leading semiconductor processes. PCBs are back on the critical path of the design cycle due to massively increasing complexity and high performance design challenges.

Some would say that selecting the right EDA vendor and tool-set for FPGA and PCB design used to be relatively simple compared to SoC. That’s no longer the case. Designing programmable platform based devices and complex boards will soon involve many of the tools and team based methods that have until now been exclusive to SoC. EDA vendor considerations and measurements will need to go far beyond the traditional focus of the point tools.

As the only EDA vendor offering ASIC, FPGA and PCB solutions Mentor Graphics has the broadest insight into the requirement of all markets. The mutual success we enjoy with our customers is based on offering far more than just great technology. In this session we’ll look at the evolution of EDA and the associated wants and needs of designers. We’ll review some traditional metrics used by our customers but go further to discover how Mentor understands the vendor selection issues beyond the core product that have made us a leader in European EDA.

Presenter:
Wesley Ryder
Technical Director Europe, Mentor Graphics Corp.
Verisity Design, Inc.

Improving Shareholder Value by Separating Verification from Design

The semiconductor industry continues to strive to manage the ever increasing risk of leaving a corner case bug that becomes the next front page story for EETimes. With cost of failure fast becoming a common agenda point in many semiconductor board room meetings around the world, how can you deliver to the ever growing demands of increasing shareholder value?

Managing scarce resources to deliver sustainable competitive advantage is the platform upon which most of today’s strategic thinking is built. Yet in the complex world of semiconductor product design we continue to see the promotion of the „jack of all trades“ designer in the false belief that it actually reduces costs.

Separating verification from design is a natural evolution to the necessary specialization that has become functional verification today. Why do accounting regulations demand that you employ armies of auditors to review your end of year accounts? When, not so many years ago, you could get away with your own accountants completing this function.

Auditors are much the same as verification engineers. They are approaching the problem from a completely different perspective. They do not come with the cognitive incompetence of „I know that’s right, because I produced it!“ The global company graveyard is littered with the tomb-stones of many household names that have made this mistake, Enron included.

In this presentation, Verisity will deliver a solution to provide unique value that can be generated when you separate the concerns of functional verification from design. Reducing the cost of failure risks and significantly improving the effectiveness of your scarce engineering resource by automating the process of verification itself.

Presenter:
Coby Hanoch
Senior Vice President of Sales,
Verisity Design, Inc.

December, 9th 2004
09.00 am - 12.00 am
Room: St. Petersburg
Magma Design Automation, Inc.

Yield and Manufacturability: the Fourth Dimension in Design Optimization

Manufacturing process control has significantly improved, however, the relative weight of process variability is increasing, thus reducing the benefits expected from technology scaling. Methodologies are now needed to design robust circuits that do not rely on impossibly tight process control, as well as, to improve circuit manufacturability.

Post-layout processing such as RET and CMP-fill are already in use today to render circuits more manufacturable, however larger impact and faster turnaround time can be achieved if yield and manufacturability become the fourth dimension in the design optimization space. This approach brings manufacturability into the IC Design flow and requires an integrated design environment to enable the desired trade-off between all circuit metrics concurrently (timing, power, noise, area AND yield). This “Manufacturing-Aware” approach should address both functional and parametric yield loss and should complement existing post-layout verification and processing techniques.

To ensure high parametric yield, process and environmental variations have been traditionally taken into account by using conservative safety margins on top of a deterministic design flow. However, this approach is too conservative and is no longer feasible. Statistical timing analysis and optimization will be needed not only to provide a performance boost, but also to allow a more flexible performance/yield trade-off. In addition, to reduce functional yield loss, yield-driven approaches will be required, e.g. synthesis for yield and critical-area-driven wire optimization.

Presenter:
Ed Huijbregts
VP Physical Synthesis
Magma Design Automation, Inc.

EDA Lounge

A new element at the edaForum04 is named “EDA Lounge”. Aiming to create an area for communication in a relaxed atmosphere, the EDA Lounge will be a meeting place inviting to sit down and talk to colleagues, partners and company representatives. The EDA Lounge will accompany the whole event.
Social Event

Follow our invitation to a culinary evening in an impressive surrounding. A delightful menu of typical Saxonian specialities is waiting for you. In between you can take a beautiful view on the river Elbe from Bruehl’s terrace. Enjoy a communicative event accompanied by two fabulous artists:

Christian Dirr – the comedy juggler – and Sebastian Matz (piano) guarantee for an unforgettable evening with comedy, music, artistry and fiery emotions.

Christian Dirr plays with bludgeons, balls and torches as well as with the laughing muscles of his spectators. His quick and charming word joke as well as the eye-winking game with the audience are the recipe for success of the turbulent show. A strange journey by comedy and juggling – a show with much spontaneous improvisation.

December 9th, 2004
Dresden, the capital of Saxony and the former residence of the Wettin dynasty, is a city of art and culture with magnificent buildings, many museums of world class as well as venues and ensembles with a rich tradition of theatre and music.

No book about the history of architecture can miss mentioning the Dresden Zwinger. The Frauenkirche, Semper Opera House and Royal Palace as well as many other historical monuments and ensembles determine the image of the city.

In December, it is a must to visit the famous »Striezelmarkt«, the oldest German Christmas fair, which attracts thousands of visitors every year.

Dresden has built up a reputation as a location for semiconductor business, where several companies established new locations. Additionally, with the new mask technology center AMTC, the co-operating companies have built the most modern plant of its kind world-wide, which is a model for further investments in nanoelectronics.
The Hilton Dresden, located in the heart of the Old Town next to the Frauenkirche, is situated on Bruehl’s Terrace. The Semper Opera House and the world renowned Zwinger are within walking distance. The piers of the world’s largest and oldest paddle steamer fleet are next to the hotel.

The edacentrum has arranged the following special room rates for attendees, valid during the edaForum04, available only with bookings by fax or phone.

Single room, standard 130 € incl. breakfast
Single room, classic 160 € incl. breakfast

Please book your room until October 27th, 2004 and mention “edacentrum” as keyword. After October 27th, the fixed quota of rooms for the edaForum04 is closed. We recommend early booking because the Hotel will be booked up very quickly for December, because of the famous Christmas fair.

The booking form can be found in this booklet. All participants are kindly asked to make their hotel reservations directly to:

Hilton Hotel Dresden

An der Frauenkirche 5
01067 Dresden
fon: +49 351 8642-0
fax: +49 351 8642-889

www.dresden.hilton.com
Registration

<table>
<thead>
<tr>
<th>Registration:</th>
<th>until</th>
<th>after</th>
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<tbody>
<tr>
<td>for edaForum04</td>
<td>Sept 25th</td>
<td>Sept 25th</td>
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<tr>
<td>edacentrum members</td>
<td>435 €</td>
<td>493 €</td>
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<tr>
<td>Non-members</td>
<td>870 €</td>
<td>928 €</td>
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(Prices include 16 % VAT)

The registration form can be found in this booklet.

The edaForum04 participation fee includes forum, social event, field trip, 2x lunch, conference beverages and conference documents. This is an all-inclusive package. The items are not available separately.

For edaForum04 the acceptable forms of payment are check, bank transfer, and credit card (Master, VISA or AMEX).

Registration Deadline: November 3rd, 2004

Please reserve yourself a place at the edaForum04 and book your room in time, because afterwards we cannot guarantee vacancy (cf. accommodation). Registrations after November 3rd will be charged with an additional fee of 50 €.

To register, mail or fax the registration form to edacentrum.

edacentrum e.V.
edaForum04 Registration
Schneiderberg 32
30167 Hannover
Germany

fax: +49 511 762 19695

Registrations are processed in a first-come-first-serve manner. Confirmation receipts will be sent via email if an email address is provided. Otherwise, confirmation letters are mailed within 7-10 business days of processing. Please review your registration receipt for accuracy.

The registration desk at the edaForum04 will be located on the 1st floor in the Piano Bar area.

December 9th -10th, 2004
Registration

Registration hours during edaForum04:

December 9th, 2004 08:30 am – 04:00 pm
December 10th, 2004 08:30 am – 09:30 am
12:30 pm – 02:00 pm

Cancellation

Cancellation (only written request) is possible free of charge until November 18th, 2004. Until November 24th, 2004, half of the fee is raised. Thereafter the entire amount becomes due. An agency of the announced participant can be named at any time.

Information KPN/CVV2/CVC2 of credit cards

The so-called “card-verification value” (CVV2) or “card-verification code” (CVC2) has been added to the rear of the card to help improve security in the remote-transaction sector. We need to have this code for a successful transaction. The value can be found in the signature field, following the printed replica of the credit card number embossed on the front of the plastic. The value is only printed and is not contained in the magnetic-stripe data (in case of American Express cards, the CVV2 is a 4-digit value to be found half way down the right-hand side of the card).

see http://www.edacentrum.de/edaforum/04registration.html

EDA Achievement Award

The award is conferred by the edacentrum to award special research or development efforts in the area of EDA in Germany; especially efforts which have been funded by the German BMBF funding program Ekomplass (design platform for complex applied systems and circuits in microelectronics).

December 10th, 2004
Field Trip

Advanced Mask Technology Center, Dresden
Advanced Micro Devices, Inc., DuPont Photomasks, Inc. and Infineon Technologies AG have jointly established the Advanced Mask Technology Center (AMTC) in Dresden.

Its mission is to develop technology and deliver R&D masks with reasonable costs and cycle times by giving technology the highest priority. Its strategy is to focus on E-Beam and EUV Laser technology development in close cooperation with the AMTC partners.

For the production process AMTC uses methods like laser writing, e-beam writing, resist development, dry etch, optical and SEM measurements, laser and ion beam repairs, ion induced gas deposition repairs and light scattering measurements.

We offer a field trip to the AMTC which gives an insight into the mask center itself and offers the opportunity to get first-hand information about the joint venture, its vision and strategy, given by representatives of the AMTC, AMD and Infineon.

The tour will end at the Hilton Hotel, approximately at 5.30 pm. You may also leave from the AMTC at about 5:00 pm and go directly to the nearby airport. http://www.amtc-dresden.de
GENERAL INFORMATION

Sightseeing

Sightseeing Tours
The “Stadtrundfahrt Dresden” offers various sightseeing tours in different languages partly combined with the possibility to visit the Frauenkirche, “Pfunds Molkerei” etc. Original double-decker busses are a perfect way to get to know the fascinating city of Dresden. Within a 1.5-hour tour you will pass all the famous places of interest like the Dresden Zwinger, Semper Opera House, Royal Palace and the bridge named “Blue Wonder”. A special evening tour offers you the experience of Dresden at night with its impressive illumination.

www.stadtrundfahrt-dresden.de/index.htm

Frauenkirche

Between 10 am and 4 pm you have the opportunity to take part in an hourly guided tour (german language) through the recently reconstructed Frauenkirche. The tour takes 45 minutes and gives an insight in the history and the reconstruction of the famous monument. http://www.frauenkirche-dresden.org/

Museums
Dresden’s most famous museums of art are the Old Masters Picture Gallery with Raffael’s Sistine Madonna, the New Masters Picture Gallery with important works from the Romantic period to the present day and the “Grünes Gewölbe” (Green Vault) with most valuable German collection of works of applied arts. http://www.skd-dresden.de/de/info.html

December 9th - 10th, 2004
GENERAL INFORMATION

Striezelmarkt
The Dresden Christmas fair is one of the oldest Christmas fairs in Germany. It has its name from the Dresden stollen cake – colloquially named “Striezel” – which has been sold since the early 16th century. The Striezelmarkt offers a big variety in woodcraft from the Erzgebirge like pyramids and nutcrackers, ceramics from Lusatia, Christmas tree decorations, textiles and Christmas candles as well as all kinds of delicacies. A special attraction on the Christmas fair is the 14 meter tall Christmas pyramid. It is the biggest one of the world, decorated by 42 wooden figures.

Medieval Christmas fair in the Stallhof
In the midst of the historic stalls of the Stallhof this historic Christmas fair offers an insight in the medieval professions of instrument builders, silver smiths, carpenters, candle makers, etc. Artists, musicians and story tellers in historic cloths guarantee a rustic atmosphere as well as the offers of open fire roasted pig, mead and home-made apple juice stand for good taste.

Volkswagen Transparent Factory
Volkswagen has built an impressive transparent factory for handcrafted cars located in the middle of the city of Dresden. At the Transparent Factory, guests will embark on a fascinating journey into the world of Volkswagen. Through a captivating array of multimedia shows, live demonstrations, hands-on exhibits and visual displays, guests will be given an unprecedented and highly entertaining emersion into the cutting-edge technology and old world craftsmanship of one of the world’s great automotive brands.

December 9th -10th, 2004
The edacentrum e.V. is an independent association dedicated to the promotion of research and development in the area of electronic design automation (EDA). Its main role is to initiate, evaluate and supervise EDA R&D projects. Further by encouraging basic research projects and EDA networks, it bundles and reinforces the EDA expertise of the German research community. The edacentrum actively engages in public relations in order to sensitize higher management levels, the public and the political arena about the central importance of design automation in microelectronics.

The association helps identify and define research projects on national and international level. In particular, it assists in the preparation and implementation of national and international EDA R&D projects funded by public authorities.

The edacentrum pursues the following strategic goals. It coordinates research and suggests new research topics, channels expertise into effective action and creates new and innovative networks, motivates and consults companies and research institutes in their use of new design methods, secures the processing and steady use of new design tools by assisting in EDA software commercialization, strengthens the market through international cooperation and standardization, supports the BMBF (German Ministry of Education and Research) with its expertise. At present, 45 companies are member of the edacentrum. As an association, the edacentrum e.V. is open to all persons and legal entities.

Directions to the Hilton Hotel Dresden, Conference location and accommodation (the Hotel is situated opposite to the “Frauenkirche”)

Arrival by train:
From central station take …
… a taxi/cab (approximately 10 minutes)
… the tram No. 8 to “Helleaur”, get off at stop „Theaterplatz.”
Walk along the “Augustusstraße” towards “Frauenkirche”
(5 min walk)
www.bahn.de
www.efa.de
www.dvb.de

Arrival by car:
From the north via the A4 motorway:
Leave motorway exit “Dresden-Hellerau”, then follow the signs to the city center (“Zentrum”) on the Hotel Route B (red)

From the west/south via the A4 motorway:
Leave motorway exit „Dresden-Alstadt”, then follow the signs to the city center (“Zentrum”) on the Hotel Route D, change to Hotel Route A at “Nossener Brücke”

Arrival by plane:
From airport Dresden (DRS) take …
… a taxi/cab (approximately 30 minutes)
… a train and train
Link S2 (for rental station), change at „Bahnhof Neustadt” into train No. 3 (to “Coschütz”), get off at stop „Synagoge”. Walk along “Trischmerplatz” towards “Frauenkirche”
(15 min walk)
… a rental car
From the airport via A4 leave motorway exit „Dresden-Alstadt”, and proceed as written above.

Outstanding EDA Experts
Meet outstanding EDA experts and enjoy discussing your favourite topics!

Keynotes
Listen to keynotes of Tom DeMarco, Ron Collett, Wojciech Maly, Tom W. Williams and Jaswinder Ahuja

Key Questions
Find Answers to key questions like
“EDA - Waste of money or key to success?”
“What system level languages will survive?”
“Design productivity - measure or die?”
“Do we need new design concepts in the physical hell below 90 nm?”

Company Presentations
See new solutions at various company presentations!

Social Event
Enjoy the exclusive social event with a beautiful view on the Elbe river.

Trips and Tours
Be guided to the new Advanced Mask Technology Center and take the opportunity to get first-hand information about the joint venture.
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Leave motorway exit „Dresden-Altstadt“ then follow the signs to the city center (“Zentrum”) on the Hotel Route D, change to Hotel Route A at “Nossener Brücke”

www.stadtplan.net
www.stadtplandienst.de

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… the train and train
Link S2 (to central station), change at „Bahnhof Neustadt“ into tram No. 3 (to “Coschütz”). Get off at stop „Synagoge“. Walk along “Tzschirnerplatz/ Töpferstraße” towards “Frauenkirche”
(5 min walk)
… a rental car.
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