2nd International Workshop on RISC-V Research Activities - Program

At this web page you find the programme of the 2nd International Workshop on RISC-V Research Activities. You may expand the programme for each session by clicking on the session title. You will find the detailed timetable, presentation titles and author names. If additional information like an abstract, curriculum vitae or (for attendees of the 2nd International Workshop on RISC-V Research Activities only) slides is available, a link below the presentation title is displayed.

Wednesday, February 27, 2019

19:00 - 22:00
Optional Come-Together/Dinner
Schneider Bräuhaus, Tal 7, 80331 Munich, Germany

Optional Come-Together/Dinner at the "Schneider Bräuhaus" on the evening before the workshop. This is an optional part of the RISC-V Activities Workshop for attendees who arrive already on Wednesday. Your drinks and food consumption is not included in the workshop fee.

Thursday, February 28, 2019

09:00 - 09:15
Welcome
Moderator: Daniel Müller-Gritschneder (TU München, D)

09:00 Welcome & Introduction
Slides (Access for event attendees only)

09:15 - 11:00
RISC-V-Hardware-Architecture and Extensions
Moderator: Daniel Müller-Gritschneder (TU München, D)

The Parallel Ultra Low Power (PULP) project at ETH Zurich
Frank K. Gürkaynak (ETH Zürich)
The ETH Zurich, in collaboration with University of Bologna has been working on developing novel energy efficient architectures as part of the PULP project for the last 6 years. We firmly believe in open source hardware and have made all our mature designs based on the popular RISC-V architecture available using a permissive license. Since our first release in 2016 (PULPino) we have released not only efficient implementations of 32 and 64 bit RISC-V processors but also, peripherals, busses and complete systems from simple micro-controllers to more involved multi-core and multi-cluster systems. In this talk, we will give an overview of our efforts and inform you of the latest developments and PULP based projects.

Slides (Access for event attendees only)

10:45 Discussion Round
11:00 - 11:15
COFFEE BREAK

11:15 - 12:15
RISC-V LLVM Compiler
Moderator: Wolfgang Müller (UPB)

Building a production-ready RISC-V LLVM toolchain
Alex Bradbury (lowRISC CIC)

"This talk will describe the current status of the upstream RISC-V LLVM backend, its implementation approach, and history. We will discuss the steps taken to evolve it towards a production readiness as well as efforts to enable downstream customisations and support for novel instruction set extensions. Alex Bradbury is primary author and code owner for the upstream RISC-V LLVM backend. lowRISC CIC is a not-for-profit with a mission to support open source hardware designs and the related ecosystem, and have driven the development of the RISC-V LLVM backend thanks to financial support from members of the RISC-V ecosystem."

Slides (Access for event attendees only)

12:00 Discussion Round

12:15 - 13:30
RISC-V and Hardware Security
Moderator: Wolfgang Müller (UPB)

Towards Reliable and Secure Post-Quantum Co-processors based on RISC-V
Tim Fritzmann (Technical University of Munich)

Increasingly complex and powerful Systems-on-Chips (SoCs), connected through a 5G network, form the basis of the Internet-of-Things (IoT). These technologies will drive the digitalization in all domains, e.g. industry automation, automotive, avionics, and healthcare. A major requirement for all above domains is the long-term (10 to 30 years) secure communication between the SoCs and the cloud over public 5G networks. The foreseeable breakthrough of quantum computers represents a risk for all communication. In order to prepare for such an event, SoCs must integrate secure quantum-computer-resistant cryptography which is reliable and protected against SW and HW attacks. Empowering SoCs with such strong security poses a challenging problem due to limited resources, tight performance requirements and long-term life-cycles. While current works are focused on efficient implementations of post-quantum cryptography, implementation-security and reliability aspects for SoCs are still largely unexplored. To this end, we present three contributions. First, we present a RISC-V co-processor for post-quantum security, able to support lattice-based cryptography. Second, we use HW/SW co-design techniques to accelerate the NTT transformation and hash generation. Third, we perform the fault analysis of the implementation. We show that our co-processor achieves high reliability and security capabilities while preserving good performance.

Slides (Access for event attendees only)

Security Features for IoT Devices based on RISC-V
Lukas Auer (Fraunhofer AISEC)

"The IoT market is moving towards increasingly integrated devices to fit within the size requirements expected by customers. At the same time, high performance under strict power constraints is demanded, requiring the use of modern process technologies. The Universal Sensor Platform (USeP), developed by several Fraunhofer Institutes aims to achieve these requirements. It integrates a range of sensors with a RISC-V based processing system as a three dimensional System-in-Package (3D-SiP). The security architecture targets the requirements of the IoT market. Secure boot and software attestation based on the DICE concept ensure only the intended software is able to run on the device. The authenticated watchdog timer as specified by the CyReP program increases the overall resiliency of the device. Data on the device is protect through encryption using the keys provided by the key management unit."

Slides (Access for event attendees only)

13:15 Discussion Round

13:30 - 14:30
LUNCH BREAK
A Verified RISC-V based Virtual Prototype using Coverage-guided Fuzzing
Vladimir Herdt (U Bremen, D)
"Virtual Prototypes (VPs) play an important role in todays design flow by enabling early SW development. Verification of VPs is crucial as undetected errors will propagate and become very costly. The Instruction Set Simulator (ISS) is a core component of the VP. We present a verified open source RISC-V based VP (available at http://www.systemc-verification.org/riscv-vp). We employed coverage-guided fuzzing (CGF) for the verification process. In particular, CGF generates an extensive testset, which we used to compare the results of our ISS with other publicly available RISC-V ISSs. We found several new errors in each considered ISS, including one error in the official RISC-V reference simulator Spike."

QEMU Support for RISC-V - Current State and Future Releases
Peer Adelt (University of Paderborn)
It its current Version 3.1.0 QEMU supports RISC-V RV32GC and RV64GC software emulation in user and full system mode. We will first give an overview of the current state of the QEMU RISC-V implementation. Thereafter, we will present the DecodeTree tool, which will be available with the next QEMU release. DecodeTree is a code generator included in QEMU that can generate the program logic for extracting and decoding opcodes and operands from a formal instruction list of the target architecture. This enables the structured implementation of just-in-time compilations to guarantee that the QEMU implementation meets the ISA specification. As such, we completely replaced the existing RISC-V RV32GC and RV64GC implementations by DecodeTree generations in the next official QEMU release, which is expected in spring 2019. We will demonstrate the DecodeTree applications by the example of RISC-V ISA subset configurations.

Simulation of RISC-V based systems in gem5
Robert Scheffel (CommSolid GmbH)
In the domain of embedded systems, full system simulators, such as gem5, are used for fast design space exploration. The absence of this type of simulators for the RISC-V architecture limits its usability in industry and academia. This presentation discusses a solution for closing this gap by introducing the implementation of the Full-System mode in gem5 for the RISC-V architecture. Furthermore, the RISC-V Extension Parser is introduced, offering the possibility to define custom extensions.

RISC-V Core Verification with cocotb
Philipp Wagner ()
cocotb is a co-simulation framework for verification of HDL designs with Python. This talk presents the riscv-cocotb project, which provides the infrastructure for verification of RISC-V processor cores.

RISC-V Verification
Moderator: Oliver Bringmann (U Tuebingen, D)

16:40 - 17:00
Closing Notes
Moderator: Daniel Müller-Gritschneder (TU München, D)
17:00  End of Workshop
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