

RISC-V core implementation in synthesizable SystemC-RTL

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Abstract

This work in progress presents a SystemC-RTL implementation of a RISC-V core based on the PULP RISCY microarchitecture. We were aiming at a simple RISC-V core model that is easily expandable for complex models in software simulation and hardware emulation environments like SiL and HiL. Taking advantage of the SystemC flexibility, we also aimed to have a portable testbench for all design steps. First, a cycle accurate RISC-V SystemC model was created and packaged with a program and RAM memory models. The functionality of the core was validated using different programs in assembler and C, verifying the registers and memory transactions. In a second step, the model was partially synthesized using a High-Level-Synthesizer for an FPGA target. Testbench portability was proved with the obtained RTL. The model will be refined to obtain a fully synthesized block and complete the FPGA target architecture to validate the reusability of the testbench.

Biography



Juan is actually part of the Virtual Systems Development team in the Fraunhofer IIS EAS, Dresden. Currently working on system level modeling, HiL, test & validation. Electronics Engineer from the Universidad Industrial de Santander, Colombia with a Master in Microsystems and Microtechnology Engineering from Hochschule Bremen, DE. Background in embedded systems and applied electronics in the field of robotics and unmanned vehicles. Hobbies of interest Remote controlled drones, cars and planes as well motor sports.