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4th Workshop on RISC-V Activities - Program

At this web page you find the programme of the 4th Workshop on RISC-V Activities. You may expand the programme for each session by clicking on the session title. You will find the detailed timetable, presentation titles and author names. If additional information like an abstract, curriculum vitae or (for attendees of the 4th Workshop on RISC-V Activities only) slides is available, a link below the presentation title is displayed.

You may download all presentations as one single ZIP file (~9,6 MB). (Access forlogged in event attendees only!)

Thursday, December 2, 2021

09:30 - 10:40
Session 1 (Invited Talks): Towards Trustworthy RISC-V Processors for Safety-critical Applications

Moderator: Daniel Müller-Gritschneder (Technical University of Munich, D)

RISC-V is one of the hottest trends in the industry these days, with its mature software toolchain and many hardware processor providers offering implementations ranging from textbook open-source cores to high-end commercial ones. The freedom to configure and customize the RISC-V ISA in accordance to the system needs, including custom instructions, is one of its strongest appeals, making custom RISC-V CPUs an attractive choice for an unprecedented number of companies. However, the challenge of actually designing a RISC-V core with custom extensions and ensuring its correct functional behaviour is still significant, even more in environments with high safety and security expectations. In this session, we present an automated flow to generate RISC-V cores with custom extensions together with their complete verification.

09:30 **Welcome**
Wolfgang Ecker (Infineon, D)

09:40 **Keynote:**
Talk 1: Towards Trustworthy RISC-V Processors for Safety-critical Applications
Eyck Jentzsch (MINRES Technologies, D)
Biography: Eyck Jentzsch holds a Dipl-Ing. from the Technical University Ilmenau and has more than 25 years experience in microelectronics and semiconductor design. He is working at MINRES as General Manager and focuses on virtual platform modelling, development, and application as well as RISC-V IP development and verification. Prior to that he worked at Cadence Design Systems Inc. And Siemens in various full- and semi-custom as well as system level design and verification positions.

Abstract and Curriculum Vitae
Slides (Access for event attendees only)

10:10 **Keynote:**
Talk 2: Towards Trustworthy RISC-V Processors for Safety-critical Applications
Salaheddin Hetalani (Siemens EDA, D)
Biography: Salaheddin Hetalani holds a M. Sc. in Embedded Computing Systems as a joint degree from the Technical University of Kaiserslautern and Southampton University and has around 3-year experience in formal design verification. He is working at Siemens EDA as Field Application Engineer and focuses on application and development of RISC-V and bus protocol VIPs

Abstract and Curriculum Vitae
Slides (Access for event attendees only)

10:40 - 11:00
Break

11:00 - 12:20
Session 2: Safety, Fault Tolerance and Hardening
Moderator: Andreas Mauderer (Bosch, D)

11:00

STRV – A SEU tolerant RISC-V implementation
Alexander Walsemann (University of Applied Sciences Dortmund, D)
Michael Karagounis (University of Applied Sciences Dortmund, D)
Felix Schneider (University of Applied Sciences Dortmund, D)
Richard Jung (University of Applied Sciences Dortmund, D)
The STRV is a RV32-IMC RISC-V core with integrated protection against Single-Event-Upsets (SEUs). It uses triple modular redundancy (TMR) and majority voting to automatically detect and correct encountered SEUs within the core and memory. The error detection and correction is done exclusively at the hardware level. Therefore, no modifications to the executed software are required to utilize the protection against SEUs. Additional memory-mapped registers are available to get information about the number of encountered SEUs. The current implementation is a reference design that will be used for comparative studies with future designs and to evaluate the relationship between power consumption, size and redundancy. The STRV was developed for use in experimental laboratories conducting research in the field of high-energy physics. However, it could also be used in other fields exposed to ionizing radiation. First silicon is expected to arrive for initial testing in November 2021.

Abstract and Curriculum Vitae
Slides (Access for event attendees only)

11:15

The TETRISC SoC for safety critical applications
Markus Ulbricht (IHP, D)
To promote the advancement of RISC-V-processors into the safety-critical domain, we focus our investigations on reliability and resiliency. In this context, our main target is the development of a highly reliable pulpissimo-based multiprocessor platform with fault tolerance mechanisms on circuit, core and system level, resulting in a robust multiprocessor SoC that is suitable for harsh environments. In order to achieve this, we hardened certain cells, added shadow registers and quadrupled the RI5CY core, thereby forming the TETRISC SoC (TETra Core System based on RISC5). The complementary HiRel Framework Controller, which acts as an in- and output multiplexer and voter, enables the forming of different NMR subsystems between the cores. Based on the harshness of the environment extracted from radiation, temperature and ageing sensors, the system is thus able to switch between high performance, DMR, TMR or QMR mode, without interrupting the computation of the non-included cores.

Abstract and Curriculum Vitae
Slides (Access for event attendees only)

11:30

RISCV-V based AI computing platform for autonomous driving
Raphael Klink (University of Lübeck, D)
Mladen Berekovic (University of Lübeck, D)
Mark Albers (Technical University of Braunschweig, D)
Benedikt Kleinbeck (Technical University of Braunschweig, D)
Alexander Dörflinger (Technical University of Braunschweig, D)
Harald Michalik (Technical University of Braunschweig, D)
The sensors used in autonomous driving such as LiDAR, radar or camera are collecting huge amounts of data. Processing these amounts of data is costly, especially as reliability and power constraints are also important factors in autonomous driving. For these reasons a RISC-V based computing platform with redundant AI accelerators is currently developed as part of the BMBF funded project KI-PRO. In this computing platform a RISC-V processor is coupled with the NVIDIA Deep Learning Accelerator (NVDLA) as a digital AI accelerator and a RRAM based crossbar as an analog AI accelerator. The computing platform is currently implemented on two different FPGA boards for testing and further development. Currently additional fault-tolerance mechanisms are added to the computing platform to further harden it against faults.

Abstract and Curriculum Vitae
Slides (Access for event attendees only)

Extending the RISC-V LLVM backend to Support Fault-tolerant Computing
Uzair Sharif (Technical University of Munich, D)
Fault tolerance against random hardware errors can be reached by software redundancy methods, which is also known as software-implemented hardware fault tolerance (SIHFT). As compiler optimization can remove this redundancy, SIHFT methods need to be implemented in the compiler backend. In this talk we present an extension of the RISC-V 32bit and 64bit LLVM backend that implements a wide range of SIHFT methods, namely
11:45 EDDI, SWIFT, nZDC, CFCSS, RASM and a new method developed by us known as REPAIR. These methods conduct either instruction duplication (data flow hardening) or signature monitoring (control flow hardening). The backend also supports selective hardening of critical functions to generate resilient RISCV binaries. It is planned to release the project as open source in the near future.

Abstract and Curriculum Vitae
Slides (Access for event attendees only)

12:00 **Q&A**

12:20 - 13:50
Lunch-Break

13:50 - 14:20
Session 3 (Invited Talk): The eProcessor project RISC-V ecosystem
Moderator: Wolfgang Müller (University of Paderborn, D)

Keynote:
The eProcessor project RISC-V ecosystem
Nehir Sonmez (Barcelona Supercomputing Center, ES)
eProcessor is a 3-year EuroHPC-JU project (started on April 2021) that involves 10 academic/industrial partners, which aims to provide an open source European RISC-V based out-of-order processor core, accelerators and a
13:50 HW/SW stack, tailored for HPC, Bioinformatics and AI applications. In this talk, the eProcessor project and its objectives will be introduced, and a brief overview of other European efforts in the RISC-V and open hardware movements will be given.

Abstract and Curriculum Vitae
Slides (Access for event attendees only)

14:20 - 15:40
Session 4: Security, Verification and Debug
Moderator: Oliver Bringmann (University of Tuebingen, D)

Verification of RISC-V Embedded Software by Integrating Concolic Testing with SystemC-based Virtual Prototypes
Sören Tempel (University of Bremen, D)
Vladimir Herdt (University of Bremen / DFKI, D)
Rolf Drechsler (University of Bremen / DFKI, D)
In this presentation we show an effective methodology for verification of RISC-V embedded software by
14:20 integrating concolic testing with SystemC-based virtual prototypes. The integration involves extending the instruction set simulator to support concolic execution and utilizing TLM extensions to support propagation of concolic values over the TLM-2.0 bus. Our RISC-V based experiments using the RIOT operating system demonstrate the effectiveness of our approach. Using a path analyzer for spatial memory safety we found several new bugs in the network stack of the RIOT operating system.

Abstract and Curriculum Vitae
Slides (Access for event attendees only)

Applying the Four-Eyes Principle to RISC-V Processor Verification by Equivalent Program Execution
Lucas Klemmer (Johannes Kepler University Linz, AT)
Daniel Große (Johannes Kepler University Linz, AT)
We present a new verification approach for RISC-V processors which allows broadening existing test programs automatically. For a given test program our approach derives a second program that is different from the original
14:35 one but proven to be equivalent. By definition, executing both programs on the same processor has to produce equal architectural states even though the executed instructions are completely different. We demonstrate the bug-finding capabilities of our approach on the well-known VexRiscv processor. Broadening a few tests already resulted in the detection of more bugs and increased test quality.

Abstract and Curriculum Vitae
Slides (Access for event attendees only)

14:50 **Setting up a debug solution with Lauterbach Debug Hardware and Software for a custom implementation of a RISC-V core - Lessons Learned**
Zhao Han (Infineon, D)
In order to enable efficient software and firmware development for a RISC-V core with custom instructions, full-featured SW debug capabilities are mandatory. This implies not only a customized hardware implementation of an on-chip debug system (OCDS), but also an aligned debugging software stack. In particular, the integration of hardware and software is essential for a complete debug solution. In this talk, we will present first the initial setup with open-source GNU GDB, OpenOCD, and J-Link. This initial setup is sufficient for proof of concept and deepening our understanding on the specification. However, open-source components are often not up-to-date and lack support. For commercial use, we migrated our debug infrastructure towards the Lauterbach solution, which includes TRACE32, Power Debug Pro, and debug cable. In this contribution, we would like to elaborate on our activities and share the lessons we learned when moving from an open source to a commercial solution for SW debug.

Abstract and Curriculum Vitae
Slides (Access for event attendees only)

15:05 **Making an Authentication Token IC Based on the Open Titan Project**
Johann Heyszl (Fraunhofer AISEC, D)
USB security tokens are powerful and established second authentication factors. We analyzed available open source products and found severe vulnerabilities in some of the included general purpose microcontrollers. We therefore posed the question: How is a hardened microcontroller for authentication tokens made from open source designs? In this talk, we describe our efforts in modifying the OpenTitan project for this purpose. Our goals are preventing attacks as seen in the real world and simplifying ASIC fabrication. In particular, we turn the OpenTitan into a flashless design, i.e., we move the NVM off-chip, and complement it with post-quantum secure boot, rigorous isolation for cryptographic keys and authenticated debug.

Abstract and Curriculum Vitae
Slides (Access for event attendees only)

15:20 **Q&A**

15:40 - 16:00
Break

16:00 - 17:35
Session 5 - Panel: The RISC-V Software Ecosystem: Where we are and where are we going?
Moderator: Stefan Wallentowitz (Munich University of Applied Sciences, D)

Considering the youth of RISC-V, the instruction set architecture has an advanced software ecosystem. With the ever-increasing number of ratified instruction set extensions and the emergence of a variety of hardware platforms, the software ecosystem is constantly in flow and several groups work on solidifying the software ecosystem, filling gaps and improving performance. In this panel discussion we will first get an overview of the state of the software ecosystem by Mark Himelstein (CTO of RISC-V) and Philipp Tomsich (Head of RISC-V Software Task Group). After that we will discuss the RISC-V software ecosystem and where it is heading. We are seeking your questions and suggestions during the panel, and you can also send it in advance to stefan [dot] wallentowitz@hm [dot] edu.

16:00 **Panel: The RISC-V Software Ecosystem: Where we are and where are we going?**
Ingo Feldner (Bosch, D)
Andrew Fustini (Beagleboard, US)
Mark Himelstein (RISC-V International, CH)
Philipp Tomsich (VRULL GmbH, AT)
Curriculum Vitae Drew Fustini
Curriculum Vitae Ingo Feldner
Curriculum Vitae Mark Himelstein
Curriculum Vitae Philipp Tomsich

17:30 **Wrap Up**
Stefan Wallentowitz (Munich University of Applied Sciences, D)