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3rd Workshop on RISC-V Activities - Program

At this web page you find the programme of the 3rd Workshop on RISC-V Activities. You may expand the programme for each session by clicking on the session title. You will find the detailed timetable, presentation titles and author names. If additional information like an abstract, curriculum vitae or (for attendees of the 3rd Workshop on RISC-V Activities only) slides is available, a link below the presentation title is displayed.

Workshop Details: https://www.edacentrum.de/en/risc-v

Registration

https://www.edacentrum.de/en/risc-v/registration
(free of charge, sponsored by edacentrum and Scale4Edge project)

About the Workshop series: https://www.edacentrum.de/en/risc-v/trainings

You may download all presentations as one single ZIP file (~17,9 MB). (Access forlogged in event attendees only!)

Thursday, October 8, 2020

08:50 - 10:00
Session 1 (Invited Talks)
Moderator: Stefan Wallentowitz (Munich University of Applied Sciences, D)

08:50 **Welcome**
Andreas Vörg (edacentrum, D)
Daniel Müller-Gritschneder (Technical University of Munich, D)

09:00 **Keynote:**
Invited Talk: RISC-V Scale4Edge Ecosystem - Motivation and Objectives
Wolfgang Ecker (Infineon, D)
RISC-V reached its 10th anniversary this May. It evolved in this decade as a de-facto standard ISA, being widely supported by universities, the open source community, and companies. The ISA is key for compiler support and opens the door to many specializations due to its openness. As David Patterson stated: Moore's Law is over, ushering in a golden age for computer architecture. Many proven architectures and models are available, both commercial and as open source solutions. However, quality is not only a topic of verification but also a matter of followed, documented, and even certifiable processes. Safety and security put additional burden in terms of verification, development flow and documentation. Further, confidence in the use of software tools must be ensured and a seamless design flow must be established. This is where the Scale4Edge project comes into place, which is introduced in this talk.

Abstract and Curriculum Vitae
Slides (Access for event attendees only)

09:30 **Keynote:**
Invited Talk: RISC-V Software Ecosystem
Jeremy Bennett (Embecosm, UK)
In this talk, I shall provide a survey of the RISC-V Software Ecosystem, both proprietary and open source. I shall look at software tools, system libraries, operating systems, IDEs and models. I shall then explore the open source ecosystem in more detail. I shall look at the approach taken by the Open Hardware Group to grow the RISC-V open source software ecosystem away from being a part time activity by volunteers, to becoming a robust commercial ecosystem, where work is done by full-time professional specialist engineers. This transition to what Mark Himelstein, CTO of RISC-V International, has described as the "Linux model" of development, is a vital step if RISC-V is to succeed in the market place. Finally I shall return to engineering, and consider the importance of measurement in evaluating systems. I shall share my experience of Embench and how modern benchmarking is an essential tool for hardware designers, compiler developers and system library writers.

Abstract and Curriculum Vitae
Slides (Access for event attendees only)

10:00 - 10:15
Break

10:15 - 11:15
Session 2 HW, Compiler and Verification
Moderator: Andreas Mauderer (Bosch, D)

10:15 **A RISC-V based Edge Computing Platform with Interchangeable Cores Using 22FDX**
Paul Palomero Bernardo (University of Tuebingen, D)
Adrian Frischknecht (University of Tuebingen, D)
Dustin Peterson (University of Tuebingen, D)
In this talk, we will present a configurable, low-power edge computing platform for efficient sensor signal processing. The platform is composed of a RISC-V processor core, a hardware accelerator, and a distributed memory architecture with dynamic content re-allocation. Following a strict hardware/model co-design approach, we have derived an optimized low-power hardware accelerator for temporal convolutional networks using a configurable array of processing elements with optimized access to the distributed memory architecture. We have integrated different RISC-V processor cores into our edge computing platform and will present the results of two alternative core implementations in Globalfoundries' 22FDX technology.

Abstract and Curriculum Vitae
Slides (Access for event attendees only)

10:30 **Energy Efficient RISC-V Implementations in 22 nm**
Heiner Bauer (Technical University of Dresden, D)
An overview of research projects at HPSN using RISC-V processors is presented. We explain our motivations to use RISC-V and the RI5CY micro-architecture for our processing elements. The integration of the CPU and the scalability of the PE architecture is demonstrated with two example projects. A comparison shows that our chip implementations in 22 nm FDSOI technology reach state-of-the-art energy efficiency numbers.

Abstract and Curriculum Vitae
Slides (Access for event attendees only)

10:45 **A Compiler Comparison in the RISC-V Ecosystem**
Mehrdad Poorhosseini (University of Oldenburg, D)
Kim Grüttner (University of Oldenburg, D)
Wolfgang Nebel (University of Oldenburg, D)
The GNU Compiler Collection (GCC) is the traditional compiler for most embedded systems, since it supports many different instruction set architectures (ISA) in its back end. GCC has also been the first compiler that supported the RISC-V ISA. Since a while Clang/LLVM has gained more and more interest in the embedded software community. Recently, RISC-V is also supported in the LLVM back-end and maintained in the official LLVM release. In this paper we propose a benchmark environment for the comparison of compilers in the RISC-V ecosystem. We perform a comparison of GCC against LLVM for an embedded software benchmark considering compile time, size of the resulting binary, number of instructions and execution time. The results show that LLVM compiles faster in 88% of the experiments, while GCC and LLVM produce nearly the same binary size in 51% of the experiments. In 37% GCC wins and in 12% LLVM wins. In 94% of the experiments the difference between the resulting binary size in GCC and LLVM is +/- 5%. The execution time analysis shows that in 42% of the experiments GCC and LLVM have nearly the same execution time clock cycles while in 40% GCC wins and in 18% LLVM wins.

Abstract and Curriculum Vitae
Slides (Access for event attendees only)

11:00 **Efficient RISC-V Processor Verification via Cross-Level Testing**
Vladimir Herdt (University of Bremen / DFKI, D)
Eyck Jentzsch (MINRES Technologies, D)
Daniel Große (Johannes Kepler University Linz, AT)
Rolf Drechsler (University of Bremen / DFKI, D)
We present an efficient cross-level testing approach for processor verification targeting the RISC-V Instruction Set Architecture (ISA). It works by generating an endless instruction stream without restrictions on the generated instructions by evolving the instruction stream on-the-fly during simulation. An Instruction Set Simulator (ISS) is leveraged as reference model for the RTL core under test in a tightly coupled cross-level co-simulation setting. This enables a very efficient and comprehensive testing process. As a case-study we present first results on the verification of the 32 bit pipelined RISC-V core of MINRES The Good Folk (TGF) Series (the ecosystem core of the BMBF funded Scale4Edge project). Our approach has been very effective in finding several serious bugs.

Abstract and Curriculum Vitae
Slides (Access for event attendees only)

11:15 - 11:45
Breakout Session 3
Moderator: Oliver Bringmann (U Tuebingen, D)

11:15 **Introduction Breakout Session**
Oliver Bringmann (U Tuebingen, D)

11:20 **Breakout Room: HW and RISC-V HW Ecosystem**
Oliver Bringmann (U Tuebingen, D)

11:20 **Breakout Room: Verification**
Vladimir Herdt (University of Bremen / DFKI, D)

11:20 **Breakout Room: Compiler + RISC-V SW Ecosystem**
Kim Grüttner (OFFIS, D)

11:45 - 12:45
Lunch-Break

12:45 - 13:30
Session 4 Virtual Prototype (VP)
Moderator: Daniel Müller-Gritschneder (Technical University of Munich, D)

12:45 **RISC-V Models for Verification, Software Development and Architectural Exploration**
Larry Lapides (Imperas Software, US)
As RISC-V processors start to be used more and more in SoCs, industry needs to look beyond the RISC-V ISA to the requirements for use. These include a well-verified implementation, the ability to develop, debug and test software, especially early in the project, and the need to explore different implementations, including different processors, multi-hart processors and custom instructions. One common element to these requirements is a high quality model of the RISC-V cores being used. This presentation will report on the test driven development methodology used to build the Open Virtual Platforms (OVP) models of RISC-V cores (~50 different cores available in the OVP Library and provided to processor IP developers), and show how these models have been used for design verification, software development and architectural exploration.

Abstract and Curriculum Vitae
Slides (Access for event attendees only)

13:00 **RISC-V core implementation in synthesizable SystemC-RTL**
Juan Camilo Santana Miranda (Fraunhofer IIS, D)
This work in progress presents a SystemC-RTL implementation of a RISC-V core based on the PULP RISCY microarchitecture. We were aiming at a simple RISC-V core model that is easily expandable for complex models in software simulation and hardware emulation environments like SiL and HiL. Taking advantage of the SystemC flexibility, we also aimed to have a portable testbench for all design steps. First, a cycle accurate RISC-V SystemC model was created and packaged with a program and RAM memory models. The functionality of the core was validated using different programs in assembler and C, verifying the registers and memory transactions. In a second step, the model was partially synthesized using a High-Level-Synthesizer for an FPGA target. Testbench portability was proved with the obtained RTL. The model will be refined to obtain a fully synthesized block and complete the FPGA target architecture to validate the reusability of the testbench.

Abstract and Curriculum Vitae
Slides (Access for event attendees only)

A Configurable Virtual Prototyping Environment for Different RISC-V ISA Subsets
Peer Adelt (University of Paderborn, D)
13:15 A virtual prototyping (VP) platform is an execution/simulation environment that executes compiled software binaries. As such, the execution needs to be compliant to the finally targeted hardware processor. This basically requires the strict behavioral compatibility of the complete tool chain, i.e., the compiler, the instruction set execution/simulation, and the target hardware. In other words, the software should have the same behavior on the VP and on the hardware target including exceptions and interrupts. The VP simulator is typically strictly implemented along the lines of the ISA manual which is fully compliant to the hardware processor which basically guarantees a full compliance between both. The RISC-V ISA standard, however, is highly configurable with respect to different subsets like RV32I, RV32IMAC, and RV32GC. That means that the complete tool chain needs to be properly aligned for exactly matching the ISA subset of the target hardware and thus to provide a meaningful validation platform. Otherwise, errors could be masked if the compiler software attempts to execute unsupported instructions without throwing exceptions, for instance. We will present our gcc-QEMU based framework which is freely configurable for arbitrary RISC-V subsets. As such, the framework automatically adapts the software compilation and virtual prototyping to the specific ISA subset. Additionally, it can be used to investigate the impact of different ISA subsets on given software source code and C/C++ compiler, like static memory allocations and dynamic runtime analysis. Our presentation will start with a basic problem statement with some examples for unsupported instructions. Thereafter, we briefly discuss the configurability of the gcc and demonstrate how QEMU can be configured by the means of decode trees.

Slides (Access for event attendees only)

13:30 - 15:25
Session 5 (Invited Talks)
Moderator: Andreas Vörg (edacentrum, D)

Keynote:
Invited Talk: CHIPS Alliance and Western Digital's RISC-V Related Activities
Zvonimir Bandić (Western Digital, US)
13:30 We will present an brief overview of CHIPS Alliance organization, which is an open source hardware organization dedicated to open source development of common hardware IP blocks, and open source software tools for ASIC design. In the second part of the talk we will focus on Western Digital contributions to CHIPS alliance, which are RISC-V SweRV cores, OmniXtend cache coherence over ethernet protocol and work on Verilator project.

Abstract and Curriculum Vitae

Keynote:
Invited Talk: Domain-Specific RISC-V Processor without Disadvantages
Zdenek Prikryl (Codasip, CZ)
14:00 On-chip processors have been traditionally grouped into silos like MCU, DSP, GPU and application processor. Designers have relied on Moore’s law rather than special architectural changes to achieve performance improvements. With gains from Moore’s law becoming more difficult to achieve architectural alternatives are being explored. In many cases what is ideal for an application may be some combination of the traditional categories as a domain-specific processor. Creating a custom instruction set and microarchitecture has traditionally been expensive and often it has been challenging to port enough middleware and software. With the open and free RISC-V ISA, there is a great opportunity to develop a domain-specific processor without the disadvantages of a fully custom ISA. RISC-V allows not only optional standard extensions but allows custom instructions which have been proven to give performance and code density gains for cryptography, DSP and AI algorithms. By creating RISC-V cores using a processor description language, Codasip provides a straightforward way of adding custom instructions and then automatically generating the hardware and software design kits. This paper explains the benefits of custom instructions and the methodology used.

Abstract and Curriculum Vitae

RISC-V in Education
Stefan Wallentowitz (Munich University of Applied Sciences, D)
14:30 RISC-V is the perfect platform for teaching computer system fundamentals and computer architecture. It has an open and vivid ecosystem of tools and materials. This presentation gives a brief overview of RISC-V in education and academia, and highlight potentials for collaboration and joint activities.

Abstract and Curriculum Vitae

14:45 **Keynote:**
Invited Talk: Collaboration and adoption Accelerate with RISC-V International with Live Q&A
Calista Redmond (RISC-V Foundation International, US)
RISC-V is gaining momentum within industries, across domains, and around the globe. Calista will detail the growth drivers that compel collaboration and adoption, the industries gaining traction, and the outlook on the bright future of RISC-V as an open ISA of choice for existing and new workloads.

Abstract and Curriculum Vitae
Slides (Access for event attendees only)

15:25 - 15:40
Break

15:40 - 16:40
Session 6 Security
Moderator: Raik Brinkmann (OneSpin Solutions, D)

15:40 **Security Issues in Hardware/Firmware interaction – Can a formal analysis of (just) the hardware help?**
Johannes Müller (Technical University of Kaiserslautern, D)
This talk describes a formal approach to verify security with respect to transient execution attacks based on hardware property checking at the register-transfer level (RTL). The approach is based on checking uniqueness of program execution with respect to confidential information. It is therefore called Unique Program Execution Checking (UPEC). UPEC can be used to systematically detect all vulnerabilities to transient execution attacks, including vulnerabilities unknown so far. This is demonstrated at the example of several open-source RISC-V processors, including Rocketchip and Boom. We then report on our current research activities extending UPEC to detecting security issues in the functionality of hardware/firmware interaction. We present preliminary results for this class of security vulnerabilities at the example of Pulpissimo and sketch future research directions.

Abstract and Curriculum Vitae

15:55 **Security and Trust Assurance of RISC-V Open-source Cores RocketCore and OpenHW CV32E**
Sergio Marchese (OneSpin Solutions, GB)
RISC-V is leading the open-source hardware revolution. Individuals, companies, and not-for-profit organizations such as the Open Hardware Group are contributing RTL cores, simulators, toolchain software, and verification testbenches and results. Hardware security is crucial for a wide range of applications, from IoT to connected autonomous vehicles and other safety-critical systems. Open-source RISC-V cores offer both security challenges and opportunities. Processor cores provide fertile soil for the insertion of hardware Trojans. Complex pipeline implementations chasing performance, power, and area targets are a great hiding place for malicious logic, bugs, and unforeseen misuse cases. Pre-silicon RTL verification focuses on intended use cases and still misses bugs routinely. Malicious actors, on the other hand, may deliberately search for unintended behaviors and misuse cases exploitable in security attacks. Scrutiny from the broad engineering community can potentially provide a level of trustworthiness assurance that no proprietary core can match. This presentation reports on security and trust assurance contributions made for the open-source cores RocketCore and OpenHW CV32E. Using a RISC-V ISA model expressed in SystemVerilog and formal verification technology, the authors were able to detect and report security-relevant bugs and undocumented, non-standard functions.

Abstract and Curriculum Vitae
Slides (Access for event attendees only)

16:10 **Leveraging the RISC-V Ecosystem for Hardware Security: A Logic Locking Approach**
Dominik Sisejkovic (RWTH Aachen University, D)
Rainer Leupers (RWTH Aachen University, D)
The involvement of third parties in the integrated circuit design and fabrication flow has introduced severe security concerns, including intellectual property piracy, reverse engineering and the insertion of malicious circuits known as hardware Trojans. Logic locking has emerged as a prominent technique to counter these security threats by protecting the integrity of integrated circuits through functional and structural obfuscation. However, this technology has been limited in its application and evaluation to small benchmark circuits, hampering the applicability in real-world scenarios. With the introduction of easy-to-access open-source RISC-V-based processor designs and their toolchain ecosystems, the evaluation of hardware security techniques on silicon-proven designs has become ever more attainable. Based on a 64-bit RISC-V core, in this work we present a holistic framework for scaling logic locking schemes to common multi-module hardware designs, thereby showcasing an industry-ready pathway of applying logic locking in a realistic design flow.

Abstract and Curriculum Vitae
Slides (Access for event attendees only)

16:25 **RISQ-V: Instruction Set Extensions and Tightly Coupled RISC-V Accelerators for Post-Quantum Cryptography**
Tim Fritzmann (Technical University of Munich, D)
Debapriya Basu Roy (Technical University of Munich, D)
Johanna Sepúlveda (Airbus, D)
Georg Sigl (TU München, Fraunhofer AISEC, D)

Empowering electronic devices to support Post-Quantum Cryptography (PQC) is a challenging task. PQC introduces new mathematical elements and operations which are usually not easy to implement on standard processors. Especially for low cost and resource constraint devices, hardware acceleration is usually required. In addition, as the standardization process of PQC is still ongoing, a focus on maintaining flexibility is mandatory. To cope with such requirements, hardware/software co-design techniques have been recently used for developing complex and highly customized PQC solutions. However, while most of the previous works have developed loosely coupled PQC accelerators, the design of tightly coupled accelerators and Instruction Set Architecture (ISA) extensions for PQC have been barely explored. To this end, we present RISQ-V, an enhanced RISC-V architecture that integrates a set of powerful tightly coupled accelerators to speed up lattice and isogeny based PQC. RISQ-V efficiently reuses processor resources and reduces the amount of memory accesses. We present the following contributions. First, we propose a set of powerful hardware accelerators deeply integrated into the RISC-V pipeline. Second, we extended the RISC-V ISA with new instructions to efficiently perform operations for lattice and isogeny based cryptography.

Abstract and Curriculum Vitae
Slides (Access for event attendees only)

16:40 - 17:15
Breakout Session 7
Moderator: Wolfgang Müller (University of Paderborn, D)

16:40 **Introduction Breakout Session**
Wolfgang Müller (University of Paderborn, D)

16:45 **Breakout Room: Virtual Prototype (VP)**
Wolfgang Müller (University of Paderborn, D)

16:45 **Breakout Room: Security**
Wolfgang Kunz (Technical University of Kaiserslautern, D)

17:15 - 17:20
Wrap-up Session 8
Moderator: Daniel Müller-Gritschneder (Technical University of Munich, D)