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Doulos Ltd.: Challenges and Solutions for ESL Design and Verification

Company Presentation: Doulos Ltd.



"Challenges and Solutions for ESL Design and Verification"

[brief description \(pdf 718kb\)](#) ^[1]

Part1: "The Verification Maze - An Independent Perspective"

Current technology allows complex System-on-Chip devices but growth in this area is limited by problems in verifying correct functionality. EDA tools using various languages are emerging to address the verification crisis but the sudden growth of languages has itself caused confusion. We call this The Verification Maze.

This presentation will help navigate The Verification Maze. We present an overview of current tools/methods and explain the jargon. We introduce the languages and present a map of how the EDA tools, methods and languages fit together. Delegates can compare the status and maturity of the tools and languages they may wish to explore further.

Part2: "A SystemC Design Flow for ARM-based Platforms"

SystemC allows a complex system to be described at multiple levels of abstraction and systematically refined from abstract algorithm to hardware with embedded software. Debate continues around the intermediate levels of abstraction and refinement methodologies between them.

This presentation will help you understand the SystemC design issues. We describe a methodology and design flow to transform an abstract model into an ARM-based platform. We show how SystemC enables architectural exploration and performance evaluation tasks at an early stage. As the design is refined, delegates will see how the SystemC models and analysis change and at which stages AMBA compliant IP can be used.

The presentation concludes with some comments on the economic impact of SystemC, based on Doulos' experience as training providers to many major electronics businesses across Europe.

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