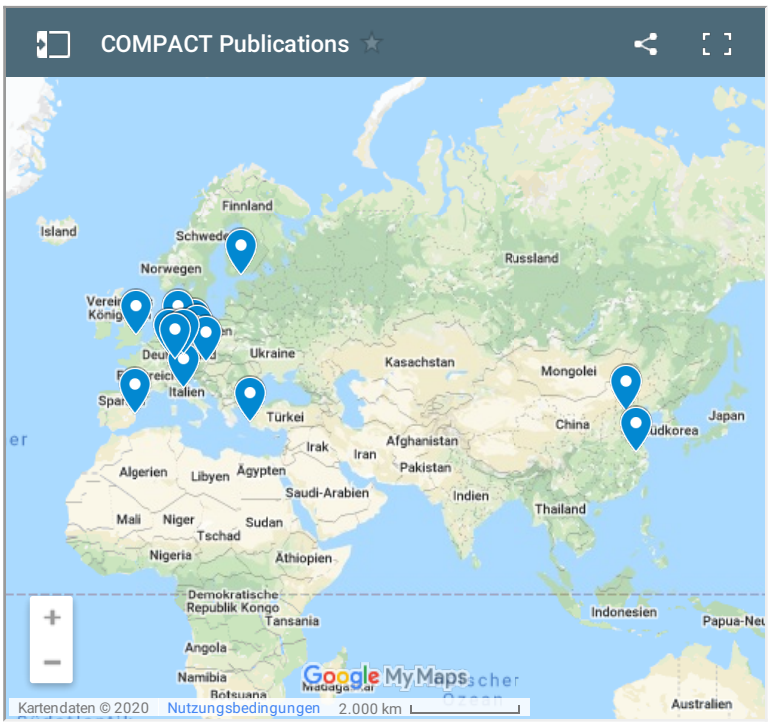
Publications

2018/12/14



1. **Rethinking Firmware Design**, W. Ecker (Infineon Technologies AG, DE), International Workshop on Embedded Software for Industrial IoT (ESIIT) at Design, Automation and Test Conference (DATE), Dresden, DE, March 23, 2018.
2. **A Structured Approach for Generating Embedded Software**, D. Keerthikumara,[1,2], W. Ecker[2,3], S. Lorenzo[2,4], M. Werner[2] ([1]U Kaiserslautern, DE, [2]Infineon Technologies AG, DE, [3]TU Munich, DE, [4]U Linz, AT), International Workshop on Embedded Software for Industrial IoT (ESIIT) at Design, Automation and Test Conference (DATE), Dresden, DE, March 23, 2018.
3. **The Third Major Revolution in Embedded Development**: P. Lieber, R. Bretz (SparxServices, AT), International Workshop on Embedded Software for Industrial IoT (ESIIT) at Design, Automation and Test Conference (DATE), Dresden, DE, March 23, 2018.
4. Invited Talk: **Bridging the Gap between Hardware Description Languages and IP-XACT**: Esko Pekkarinen, Timo D. Hämäläinen, (TU Tampere, FL), International Workshop on Embedded Software for Industrial IoT (ESIIT) at Design, Automation and Test Conference (DATE), Dresden, DE, March 23, 2018.
5. Invited Talk: **Ultra Low Power Solutions for IoT Devices**: L. Koskinen (Minima Processor Ltd., FL), International Workshop on Embedded Software for Industrial IoT (ESIIT) at Design, Automation and Test Conference (DATE), Dresden, DE, March 23, 2018.
6. **Challenges in Property Generation**, Wolfgang Ecker (Infineon Technologies AG und TU Munich, DE, edaWorkshop18, Hannover, DE, May 16, 2018.
7. **Firmware Generation: State-of-the-Art, Challenges, and New Approaches**, Wolfgang Ecker, Lorenzo Servadei, Michael Werner, Elena Zennaro (Infineon Technologies AG und TU Munich, DE), edaWorkshop18, Hannover, DE, May 17, 2018.
8. **COMPACT-Project**, W. Ecker, Infineon, DE, et al., ITEA Innovation Days in Helsinki, FI, April 2018.
9. Daniel Mueller-Gritschneder: **Extendable Translating Instruction Set Simulator (ETISS) with RISC-V Support and SystemC/TLM Pulpino Virtual Platform**, Presentation at the RISC-V Activities Workshop, Munich, DE, June 21, 2018.
10. Adelt, B. Koppelmann, W. Mueller. **Current and Future RISC-V Activities for Virtual Prototyping and Chip Design**. Presentation at the RISC-V Activities Workshop, Munich, DE, June 21, 2018.
11. Benz, J., Jung, A., Bringmann, O.: **A context-sensitive PEG-based timing model for a PULPINO-derived RISC-V microprocessor**, RISC-V Activities Workshop, Munich, DE, June 21, 2018
12. **A Machine Learning Approach for Area Prediction of Hardware Designs from Abstract Specifications**, Elena Zennaro[2], Lorenzo Servadei[2], Keerthikumara Devarajegowda[12] and Wolfgang Ecker[23] ([1]U Kaiserslautern, DE, [2]Infineon Technologies AG, DE, [3]TU Munich, DE), Euromicro Conference on Digital System Design, Prague, CZ, August 2018.
13. Rafael Stahl, Daniel Mueller-Gritschneder, Ulf Schlichtmann: **Automated Redirection of Hardware Accesses for Host-Compiled Software Simulation**, Forum on Design Languages (FDL), Munich, DE, Sept. 2018.
14. Aljoscha Kirchner [1], Jan-Hendrik Oetjens, Oliver Bringmann; **Using SysML for Modelling and Code Generation for Smart Sensor ASICs,** Forum on Design Languages (FDL), Munich, DE, Sept. 2018.

15. Daniel Müller-Gritschneder, Ulf Schlichtmann; **Extendable Translating Instruction Set Simulator (ETISS)**; Poster at ARM Research Summit, Cambridge, UK, Sept. 2018.
16. **Quality Assessment of Generated Hardware Designs Using Statistical Analysis and Machine Learning,** Lorenzo Servadei[1,2], Elena Zennaro[1,3], Keerthikumara Devarajegowda[1,4], Wolfgang Ecker[1,3], Robert Wille[2], [1]Infineon Technologies AG, Am Campeon 1-15, 85579 Munich, Germany, [2]Johannes Kepler University Linz, Altenbergerstraße 69, 4040 Linz, Austria, [3]Technical University of Munich, Arcisstraße 21, 80333 Munich, Germany, [4] of Kaiserslautern, Erwin-Schrödinger-Str. 1, 67663 Kaiserslautern, Germany, International Conference on Tools with Artificial Intelligence (ICTAI) , Volos, Greece, Nov. 2018.
17. The current status of COMPACT was presented to MdB Andreas Steier during a visit to the Infineon Campeon, 2018.
18. Bewoayia Kebianyo, Philipp Ittershagen, Kim Grüttner: **Towards Stateflow Model Aware Debugging with LLDB**, 11th Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools (RAPIDO), *Veröffentlichung Januar 2019*
19. **Bridging XML and UML – An Automated Framework**, A. Kühlwein, S. Reiter, W. Rosenstiel, O. Bringmann, International Conference on Model-Driven Engineering and Software Development (MODELSWARD), Prague, CZ, February 2019.
20. Invited Talk: **Embedded Systems Automation following OMG's Model Driven Architecture Vision**, W. Ecker[2,3], D. Keerthikumara,[1,2], M. Werner[2] ([1]U Kaiserslautern, DE, [2]Infineon Technologies AG, DE, [3]TU Munich, DE), at Design, Automation and Test Conference (DATE), Florence, IT, March 28, 2019
21. Kuhn, M., Bringmann, O.: **Source-level Power Simulation of IoT Firmware for Energy Evaluation**, Accepted for Presentation at the 2nd International Workshop on Embedded Software for Industrial IoT (ESIIT), Florence, IT, March 2019
22. Bewoayia Kebianyo, Philipp Ittershagen, Kim Grüttner: **Towards Stateflow Model-Aware Debugging using Model-to-Source Tags with LLDB**, 2ndInternational Workshop on Embedded Software for Industrial IoT (ESIIT), Florence, IT, March 2019
23. Adelt, B. Koppelmann, W. Mueller, Chr. Scheytt, B. Driessen. **QEMU for Dynamic Memory Analysis of Security Sensitive Software**, 2nd International Workshop on Embedded Software for Industrial IoT (ESIIT), Florence, IT, March 2019
24. **Proposals for IP-XACT Extensions from Embedded Controller Use Cases** Velten, W. Ecker, 2nd International Workshop on Embedded Software for Industrial IoT (ESIIT), Florence, IT, March 2019
25. Adelt, Peer; Koppelmann, Bastian; Müller, Wolfgang; Scheytt, Christoph: **Analyse sicherheitskritischer Software für RISC-V Prozessoren**. In: Workshop Methoden und Beschrei-bungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen (MBMV 2019), Kaiserslautern, DE, Apr. 2019
26. **Using SysML for Modelling and Generation of Virtual Platforms**: Aljoscha Kirchner, Jan-Hendrik Oetjens, Oliver Bringmann, Tim Kogel; Synopsys User Group (SNUG) Europe, Munich, DE, May 2019
27. Rafael Stahl, Zhuoran Zhao, Daniel Mueller-Gritschneder, Andreas Gerstlauer and Ulf Schlichtmann, **Fully Distributed Deep Learning Inference on Resource-Constrained Edge Devices,** SAMOS XIX 2019, "International Conference on Embedded Computer Systems: Architectures, MOdeling and Simulation", Samos Island, GR, July 7-11, 2019
28. **Firmware Synthesis for Ultra-Thin IoT Devices Based on Model Integration**, A. Kühlwein, A. Paule, L. Hielscher, W. Rosenstiel, O. Bringmann, International Workshop on Modeling Language Engineering and Execution (MLE), Munich, DE, September 2019.
29. **JIT-Based Context-Sensitive Timing Simulation for Efficient Platform Exploration**, A. Cornaglia, M.S. Hasan, A. Viehl, O. Bringmann, W. Rosenstiel, 25th Asia and South Pacific Design Automation Conference (ASP-DAC), Beijing, China, Jan. 2020
30. **Cyber Security Modeling: the Secure Standing Pillar for IoT**, Orsolya Nemeth (Sparx Services CE), Security in the Age of Industry 4.0 and Digitization on 20.11.2019, Vienna, Austria
    As an important milestone in the European funding project "ITEA3 COMPACT", we have developed a method that combines software and system modeling with Cyber Security Threat Modeling. In addition to identifying known threats, we are currently working on the automated fulfillment of ISO27000 requirements for secure IoT systems. Time and effort for development can thus be significantly reduced.
31. Adelt, B. Koppelmann, W. Mueller, C. Scheytt. **QEMU Support for RISC-V: Current State and Future Releases**. Presentation at the RISC-V Activities Workshop, Munich, DE, February 28, 2019
32. Koppelmann, Bastian; Adelt, Peer; Müller, Wolfgang; Scheytt, Christoph: **RISC-V Extensions for Bit Manipulation Instructions**. In: 29th International Symposium on Power and Timing Modeling, Optimization and Simulation (PATMOS), Rhodes, Greece, July 2019
33. Embedded World in Nurnberg, March 2019, **Presentation of current stage of IoT-PML**, Daniel Siegl, SSCE
34. Safety Event in Munich, July 2019, **Tutorial about „Modern Model Based IoT development"** by Peter Lieber, Richard Deininger, SSCE
35. Tutorial at TdSE (INCOSE) Event in Munich, November 2019, **Presentation of current research results in IoT domain** by Daniel Siegl, Richard Deininger, SSCE
36. **Best Paper Award**: "Neural Network-based Vehicle Image Classification for IoT Devices" by Saman Payvar, Mir Khan, Rafael Stahl, Daniel Müller-Gritschneder, Jani Boutellier and Luca Ferranti received the Best Paper Award (2nd prize) of IEEE SiPS 2019, October 20-23, 2019, Nanjing, CN
37. **A Scalable Platform for QEMU Based Fault Effect Analysis for RISC-V Hardware Architectures**, Peer Adelt, Bastian Koppelmann, Wolfgang Müller und Christoph Scheytt, UPB, MBMV, Stuttgart, DE, 19.-20.3.2020.

COMPACT ist ein ITEA3-Projekt (Referenznummer: 16018). COMPACT wird gefördert durch die Österreichische Forschungsförderungsgesellschaft FFG (Projektnummer 863828), die finnische Förderagentur für Innovation Tekes (Diary Number 3098/31/2017) und das Bundesministerium für Bildung und Forschung (BMBF) (Referenznummer: 01IS17028).

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[1] https://ieeexplore.ieee.org/search/searchresult.jsp?searchWithin=%22First%20Name%22:%22Aljoscha%22&searchWithin=%22Last%20Name%22:%22Kirchner%22&newsearch=true&sortType=newest