

MARLOW

**TUD, POLITO, UP, IMEC, CSEM, LIRMM, OFFIS
present:**

The FIFTH

MARLOW

WORKSHOP

Technical University of Budapest

Budapest, Hungary

April 29, 2005

For Information and Registration:

<http://www.lowpower.org>

Organizers:

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WORKSHOP PROGRAM

- 08.00-09.00: Registration
- 09.00-09.30: Welcome
Wolfgang Nebel, OFFIS, D
Enrico Macii, Politecnico di Torino, I
Marta Rencz, Technical University of Budapest, H
- The MARLOW Thematic Network
Rene van Leuken, Delft Technical University, NL
- 09.30-10.15: Keynote Speech 1
Low-Power MicroSystems.
Dr. Nicolas Delorme, CEA-LETI, F
- 10.15-11.00: Keynote Speech 2
High-Level Estimation and Optimization of Power and Delay in
Nano-Scaled Interconnects
Dr. Tudor Murgan, Technical University of Darmstadt, D
- 11.00-11.30: Coffee Break
- 11.30-12.30: The MARLOW Low-Power Roadmap
Dr. Johan Vounkx, IMEC, B
- Open discussion
- 12.30-14.30: Lunch
- 14.30-15.30: Short Course 1
System-Level Design for Low Power
Prof. Wolfgang Nebel, OFFIS, D
- 15.30-16.00: Coffee Break
- 16.00-17.00: Short Course 2
Leakage Power Modeling, Estimation and Optimization
Mr. Domenik Helms, OFFIS, D
- 17.00: Closing

Keynote Speech 1

Designing Low-Power MicroSystems

Dr. Nicolas Delorme, CEA-LETI, F

Abstract

With the advent of autonomous sensor nodes, low power has become a key aspect of micro-system design. This keynote focuses on the design methodologies and tradeoffs that can lead to successful low-power microsystems for sensor applications. Several practical design cases are presented and compared to the state of the art in terms of readout resolution, bandwidth and power consumption.

Keynote Speech 2

High-Level Estimation and Optimization of Power and Delay in Nano-Scaled Interconnects

Dr. Tudor Murgan, Technical University of Darmstadt, D

Abstract

The rapid evolution in process technology allows the integration of increasingly complex systems in VLSI chips operating at continuously rising frequencies. The increase in number of devices and system complexity with shrinking device features implies the use of long and tightly coupled global interconnects. Such trends generate higher delays and undesired cross-talk interference because of increasing capacitive and inductive coupling. This talk addresses estimation and optimization of power consumption and signal delay in nano-scaled on-chip interconnects at high levels of abstraction.

Short Course 1

System-Level Design for Low Power

Prof. Wolfgang Nebel, OFFIS, D

Abstract

More features and higher bandwidth needed for new mobile services consume more power than battery technology can provide. Higher performance in information processing produces more heat than cooling technology can dissipate. These trends require power aware design methodologies throughout the entire design. The largest impact on the power consumption can be achieved at the system level where the algorithms and the system architecture are defined. In this contribution a System-Level design flow and respective EDA support tools for low power designs are presented.

Short Course 2

Leakage Power Modeling, Estimation and Optimization

Mr. Domenik Helms, OFFIS, D

Abstract

In this tutorial, an introduction to the increasingly important effect of leakage power in recent and upcoming technologies will be given. The sources of leakage such as subthreshold leakage, gate leakage, pn-junction leakage and further GIDL, hot-carrier effect and punch-through are identified and analyzed separately as well as under consideration of PTV variations. Since leakage will dominate power consumption in future technologies, also leakage optimization techniques and leakage estimation approaches supporting optimizations especially at higher abstraction levels will be reviewed.